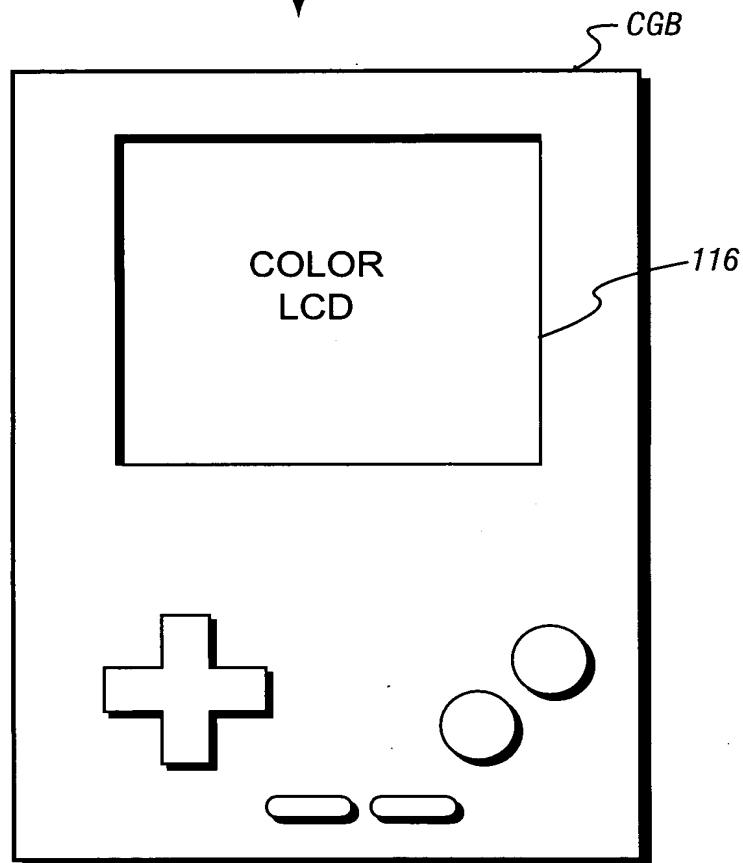


MAX. 56 COLORS ON
ONE SCREEN



COLOR DISPLAY GAME
MACHINE

Fig. 1A

Fig. 1B

158

Fig. 1C

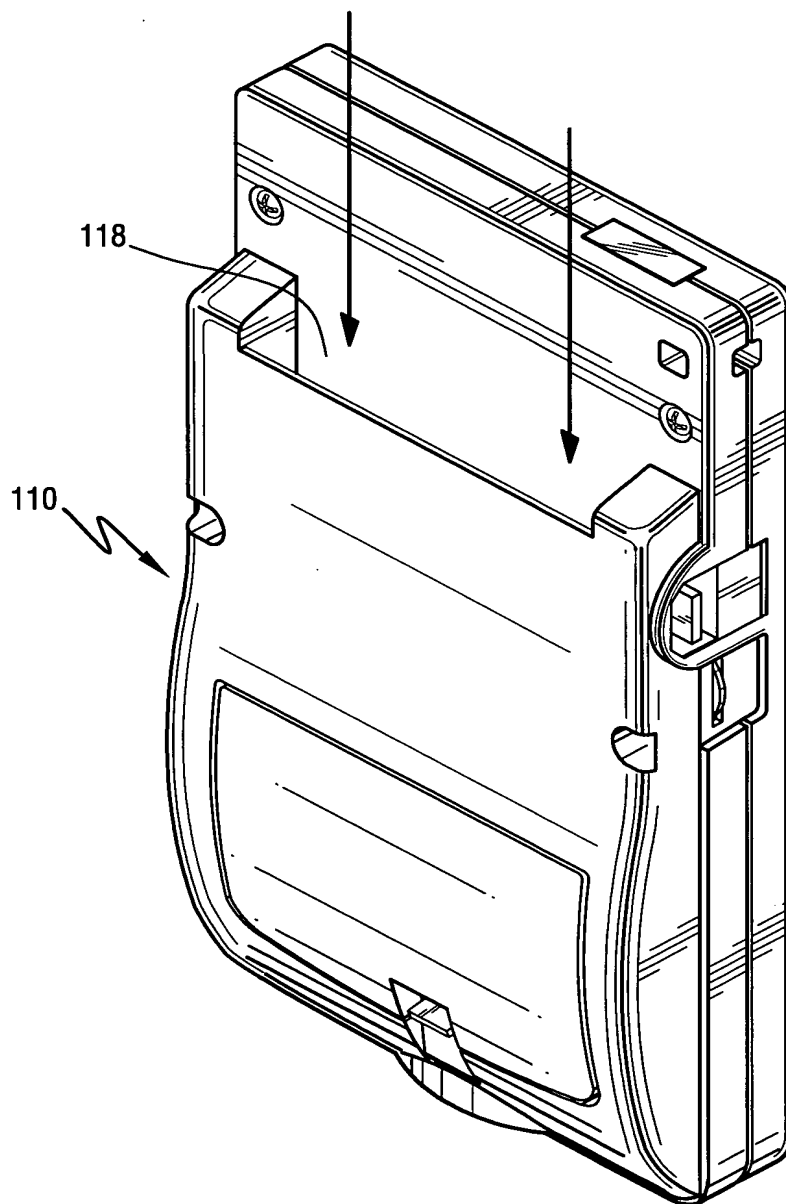
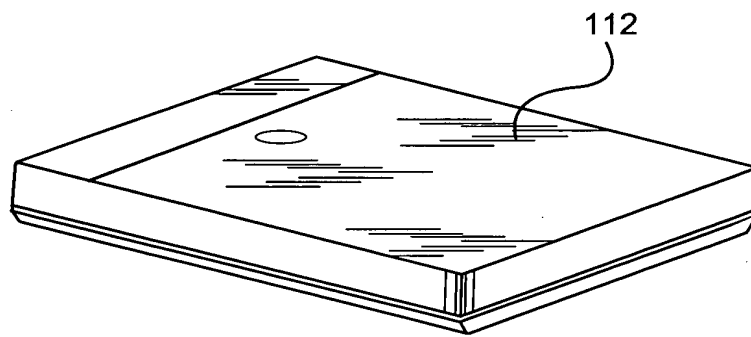


Fig. 2
(Prior Art)



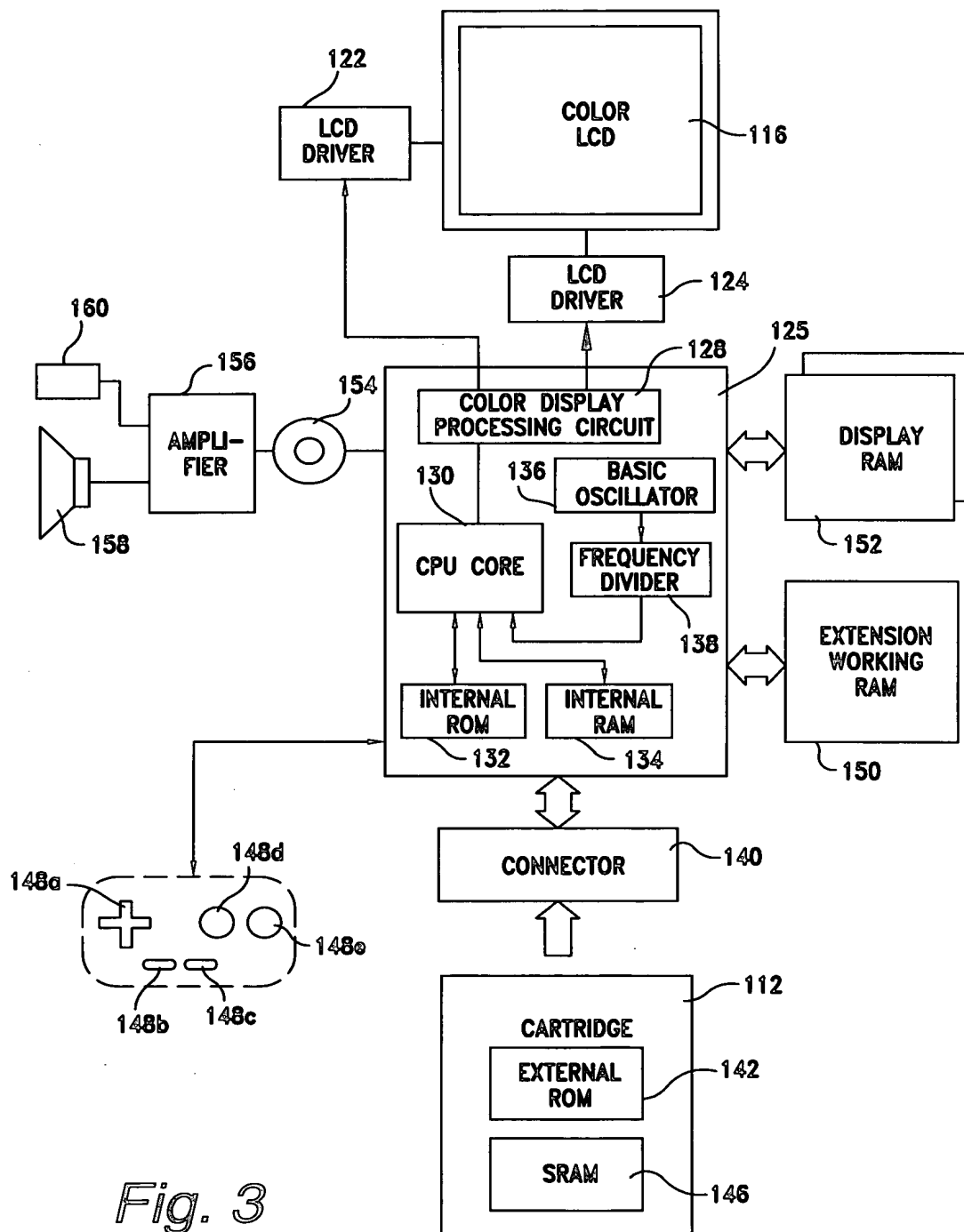
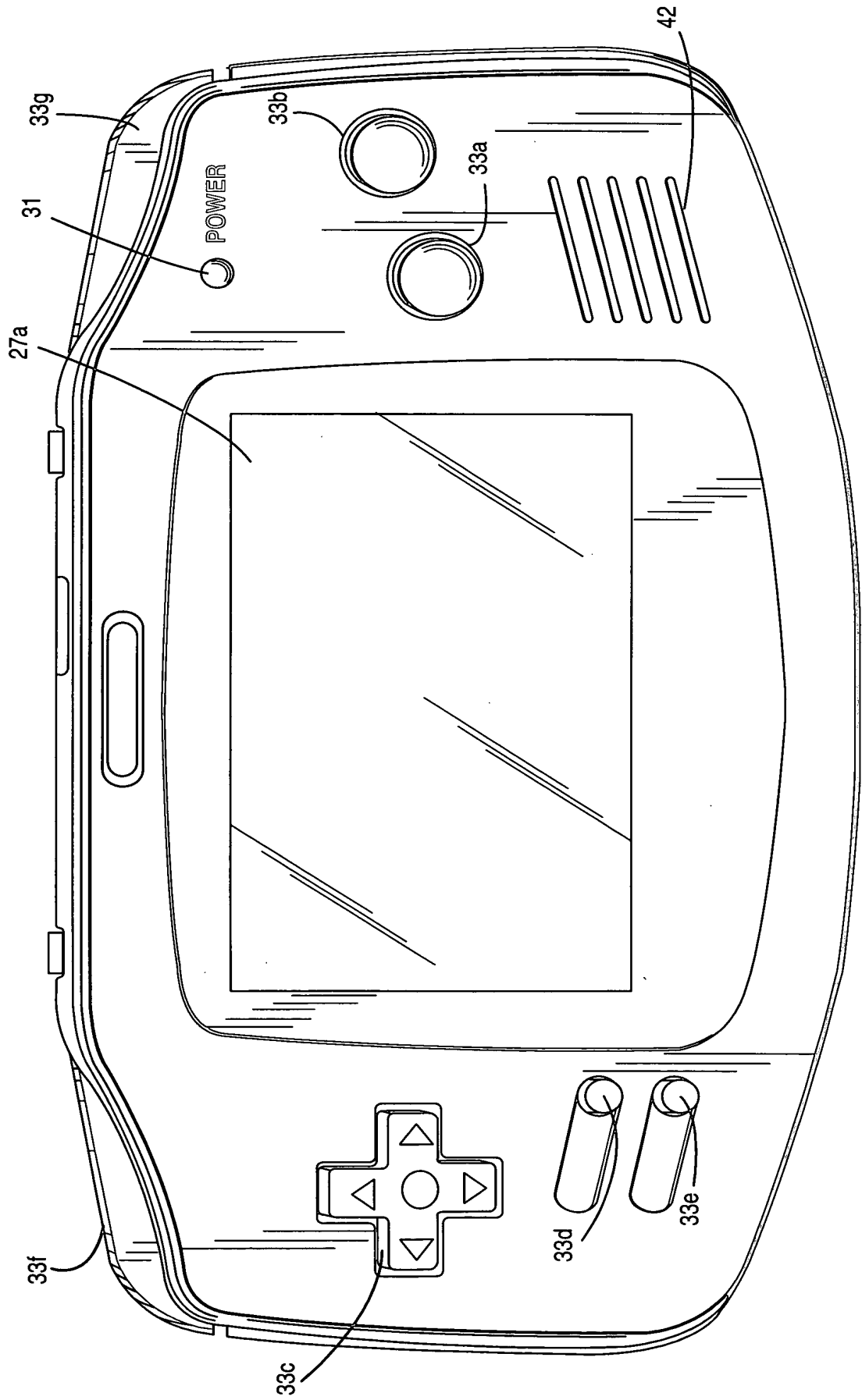


Fig. 3

Fig. 4A



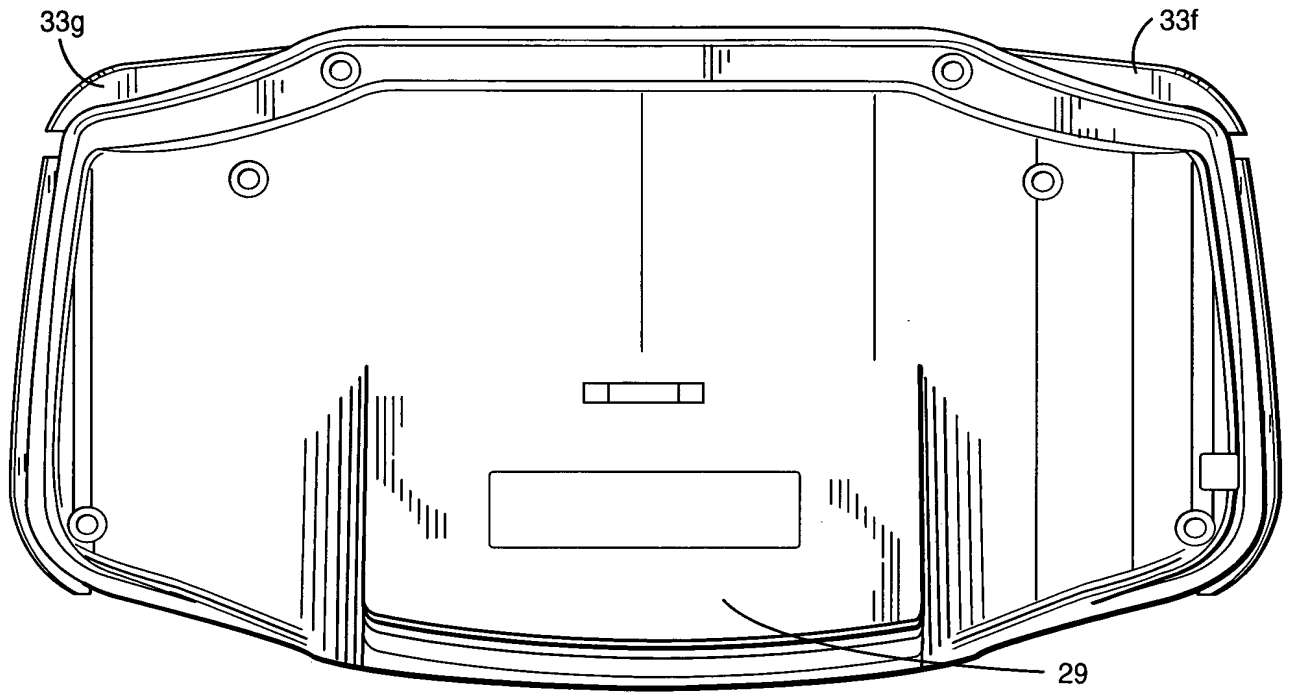


Fig. 4B

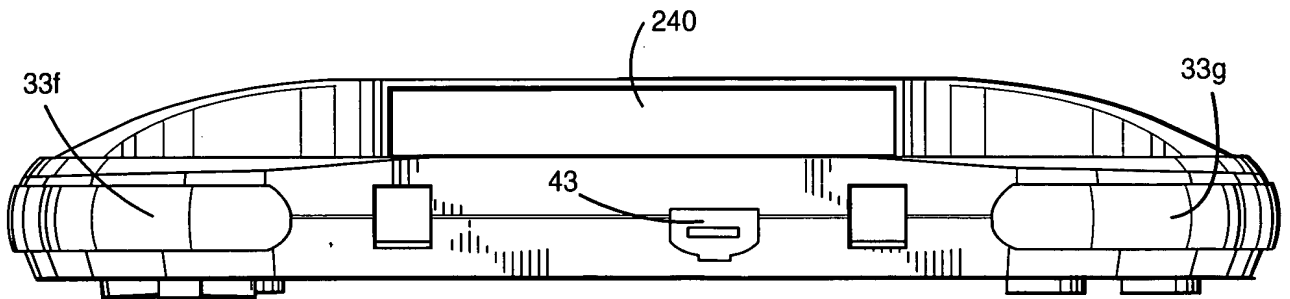


Fig. 4C

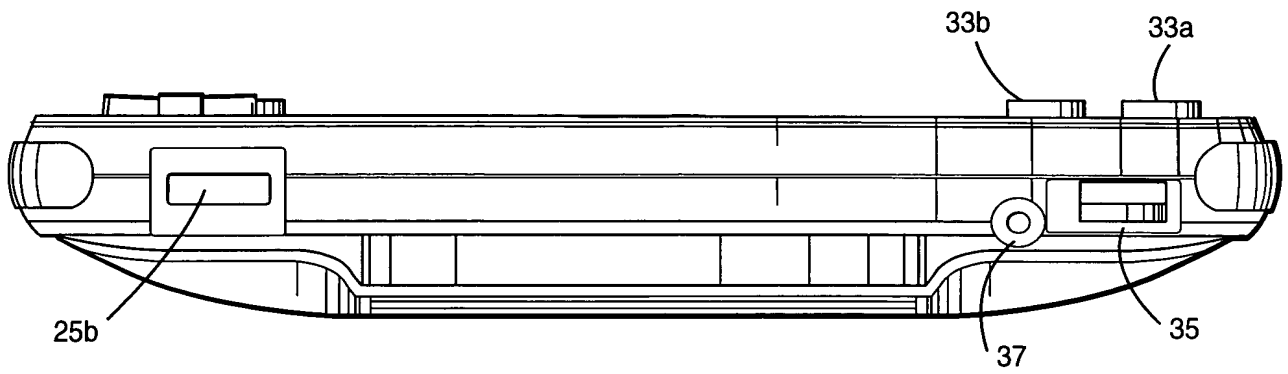


Fig. 4D

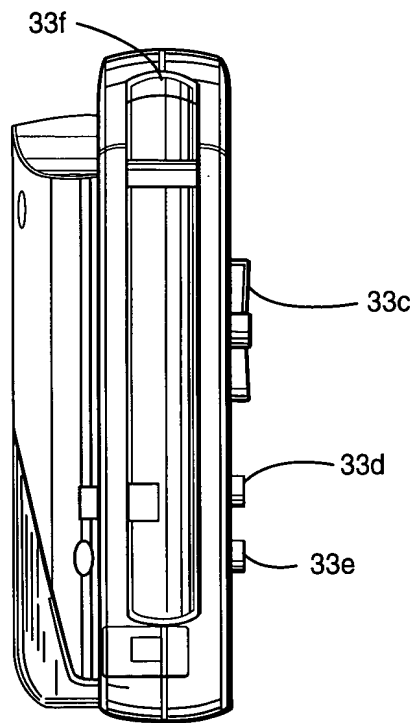


Fig. 4E

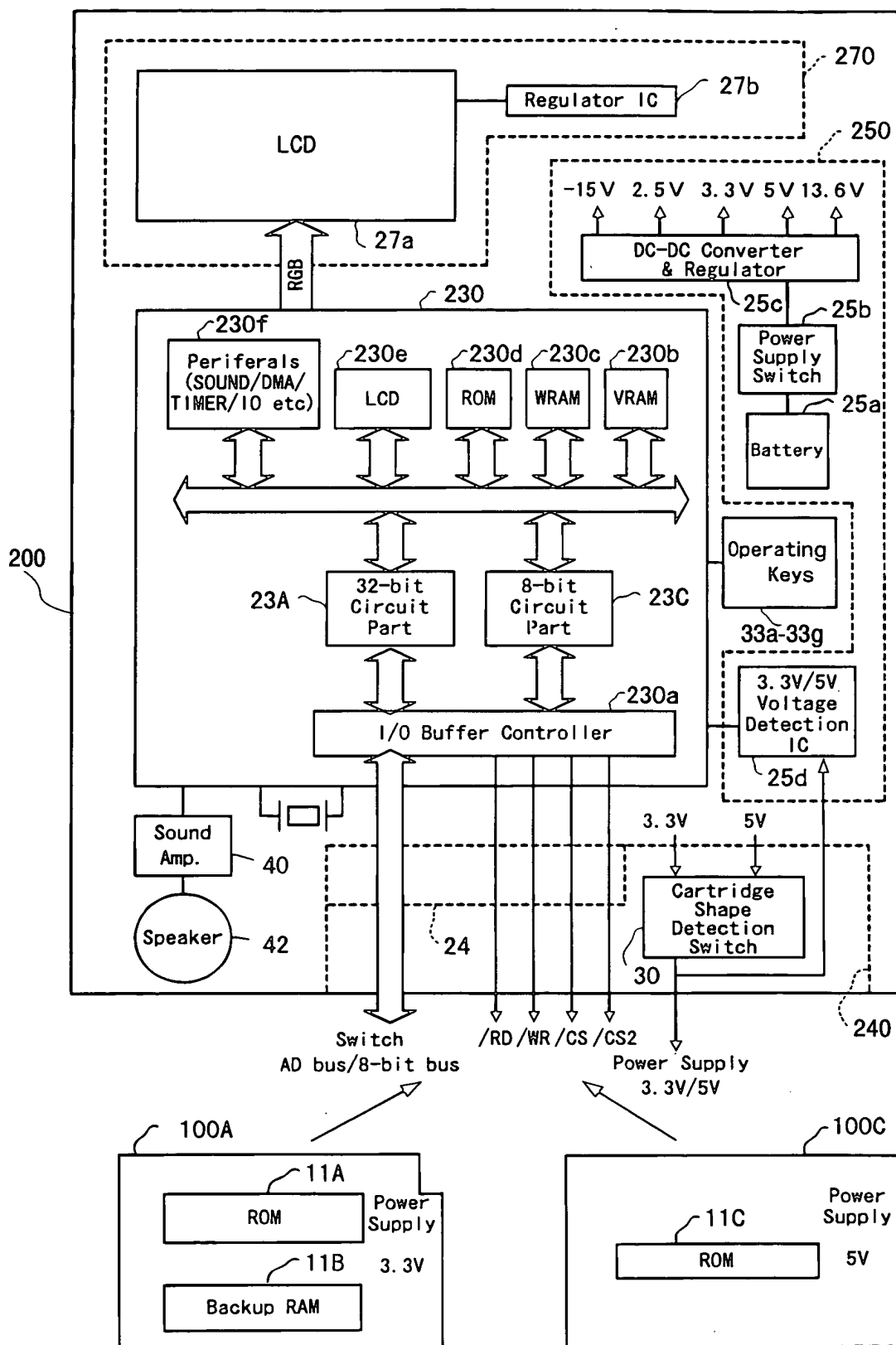


Fig. 5B

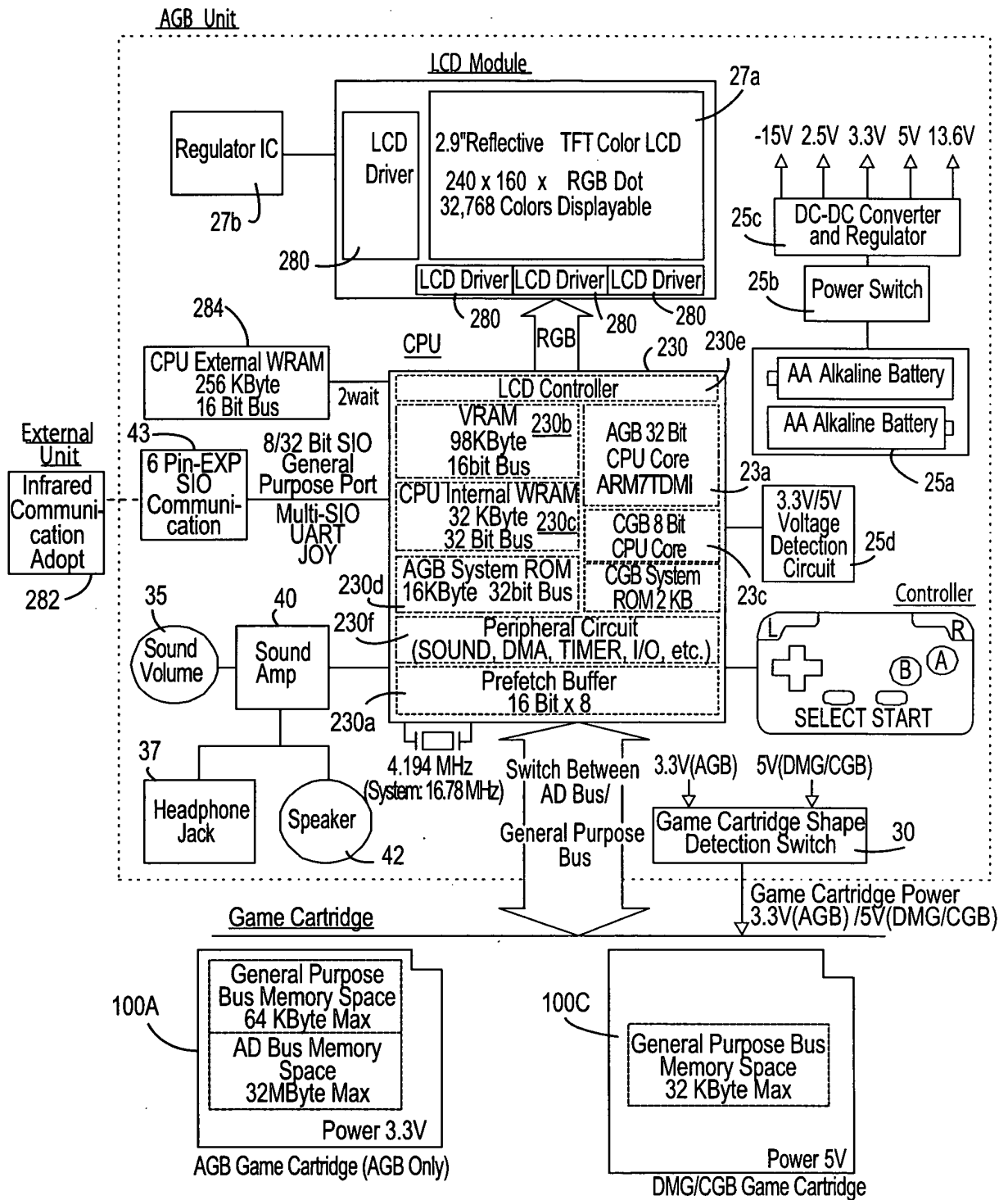
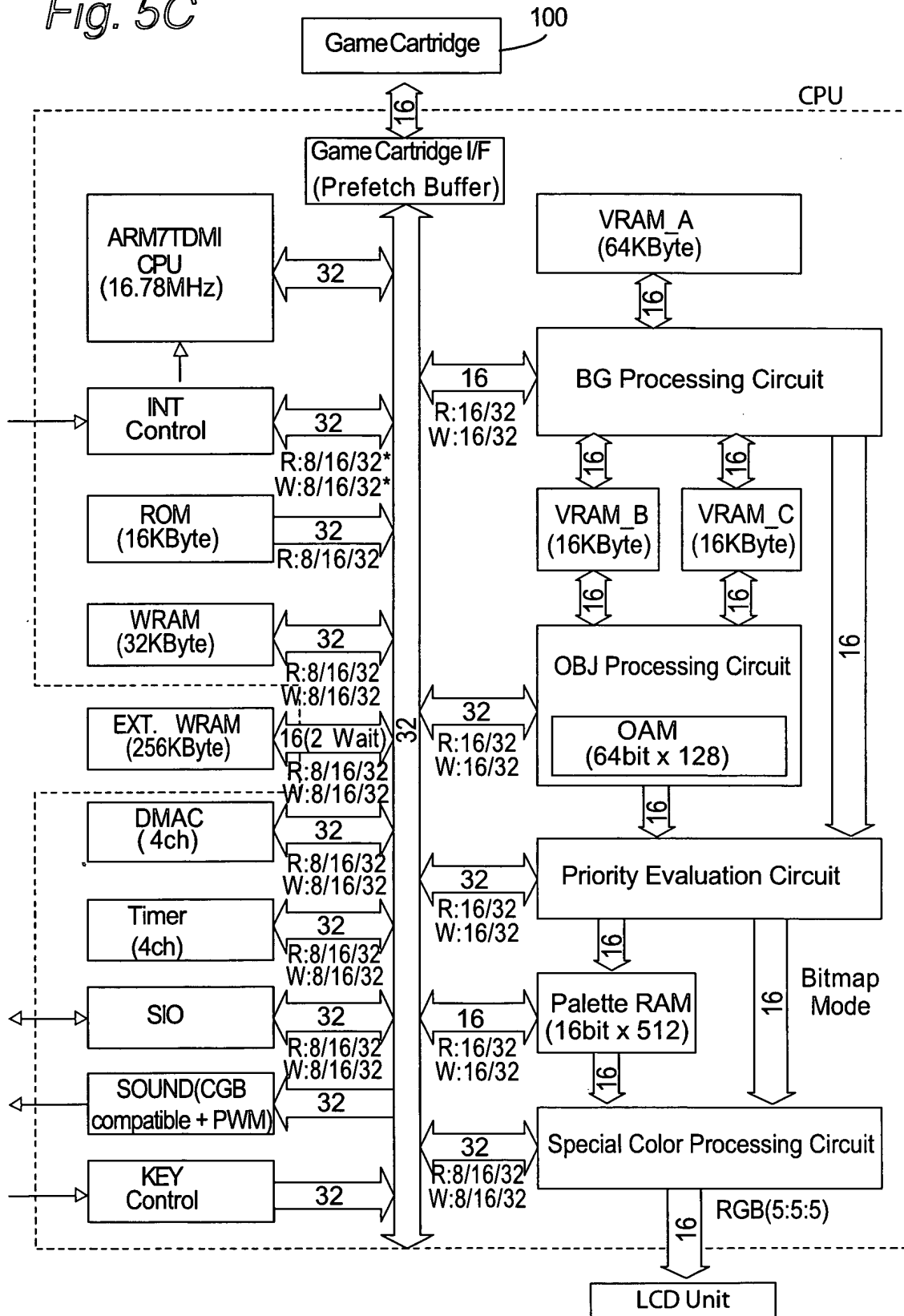


Fig. 5C



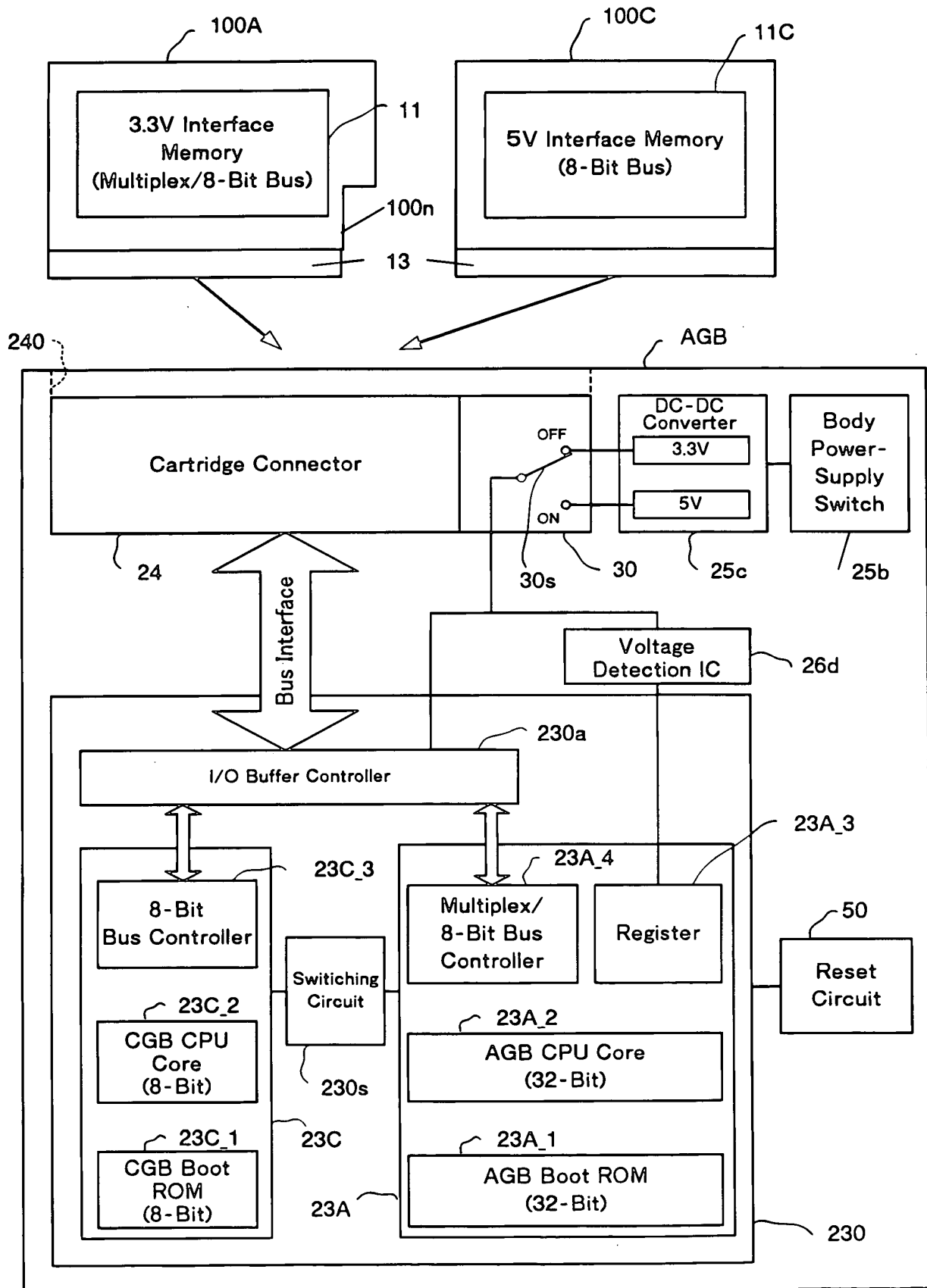


Fig. 6

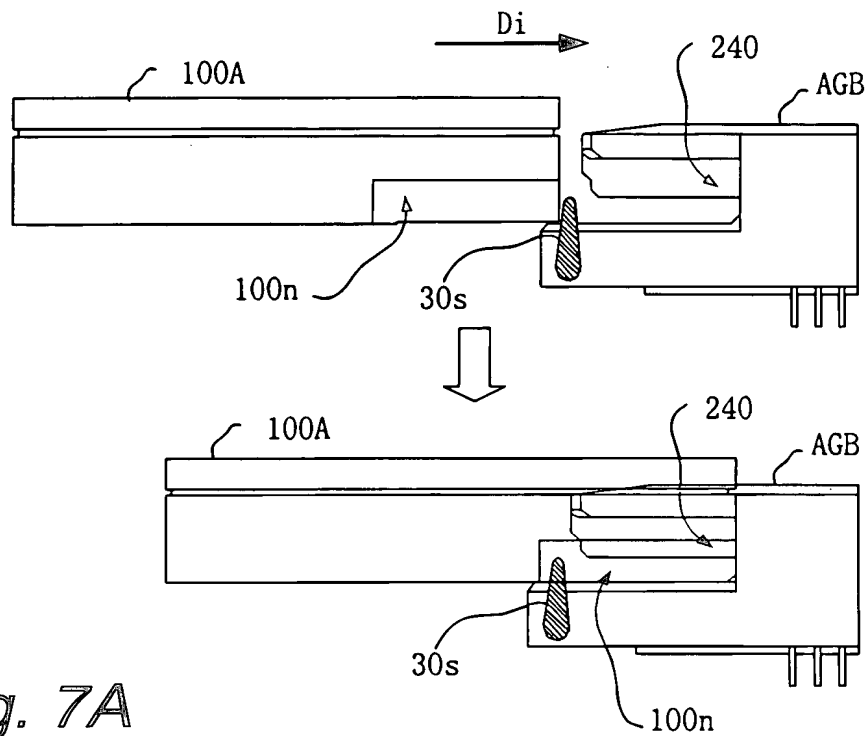


Fig. 7A

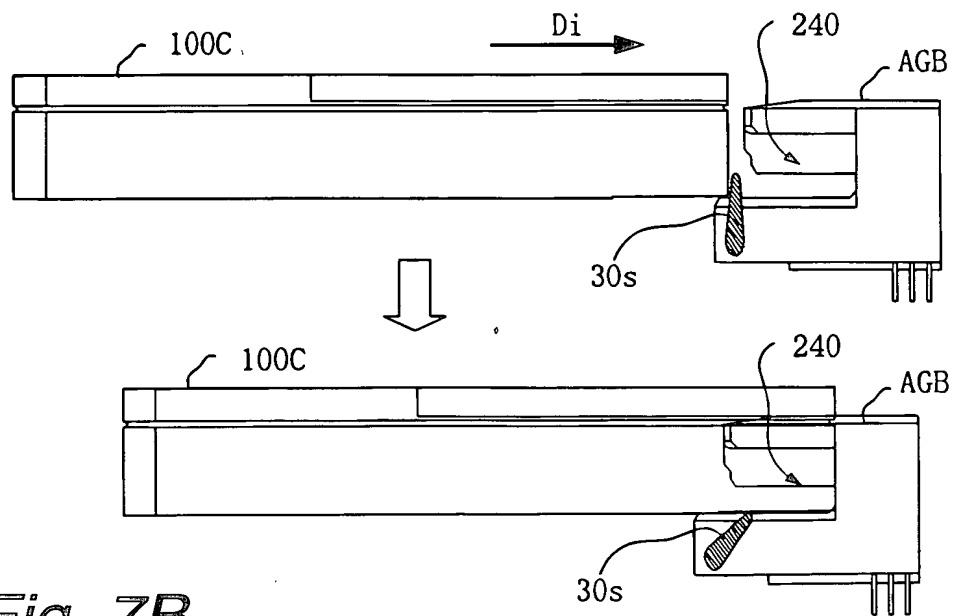


Fig. 7B

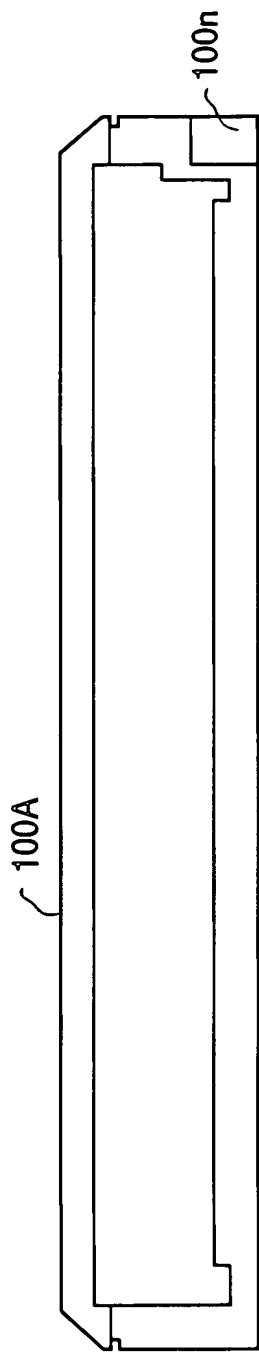


Fig. 8A

100C

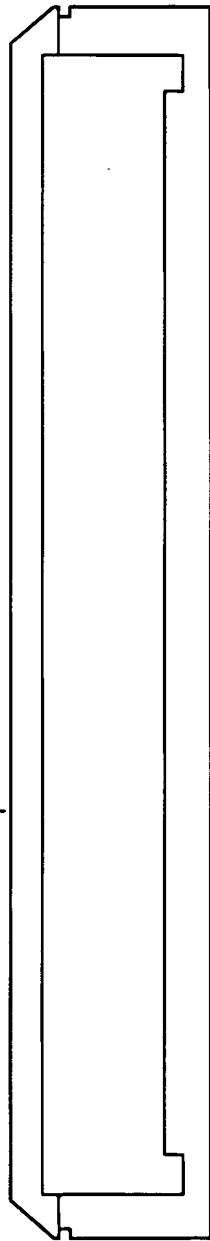


Fig. 8B

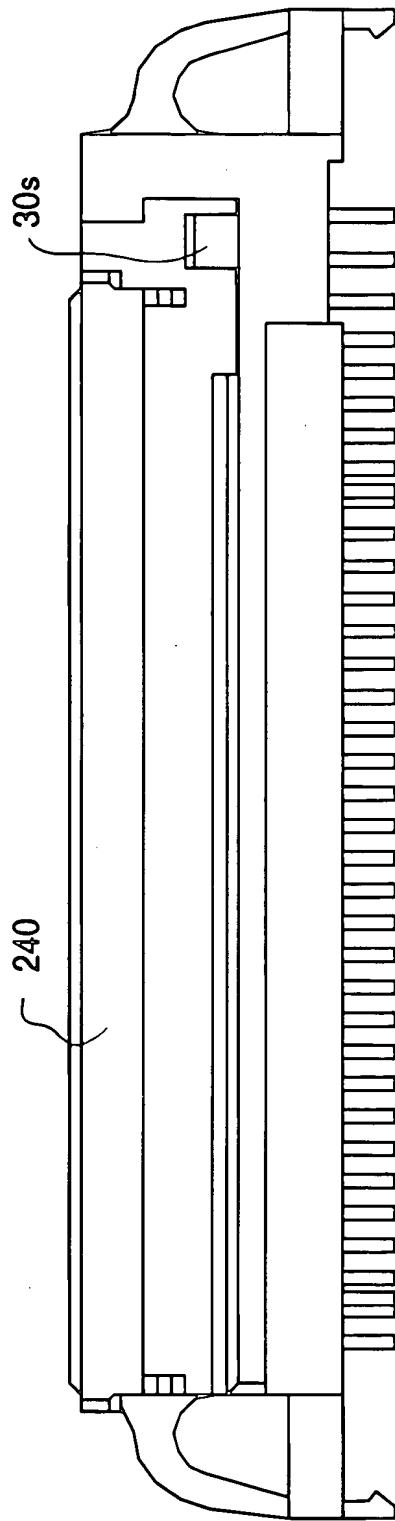
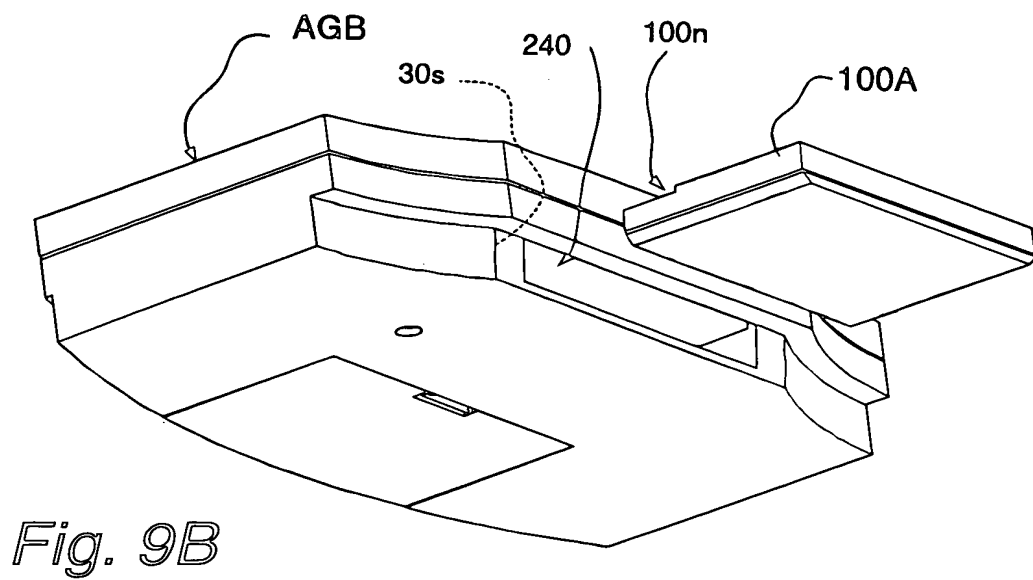
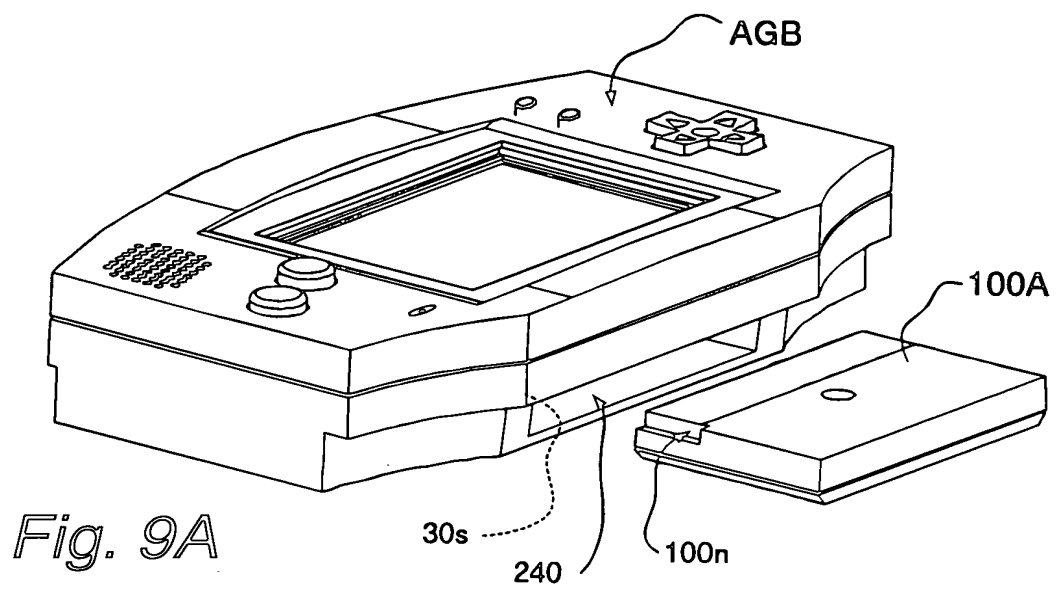
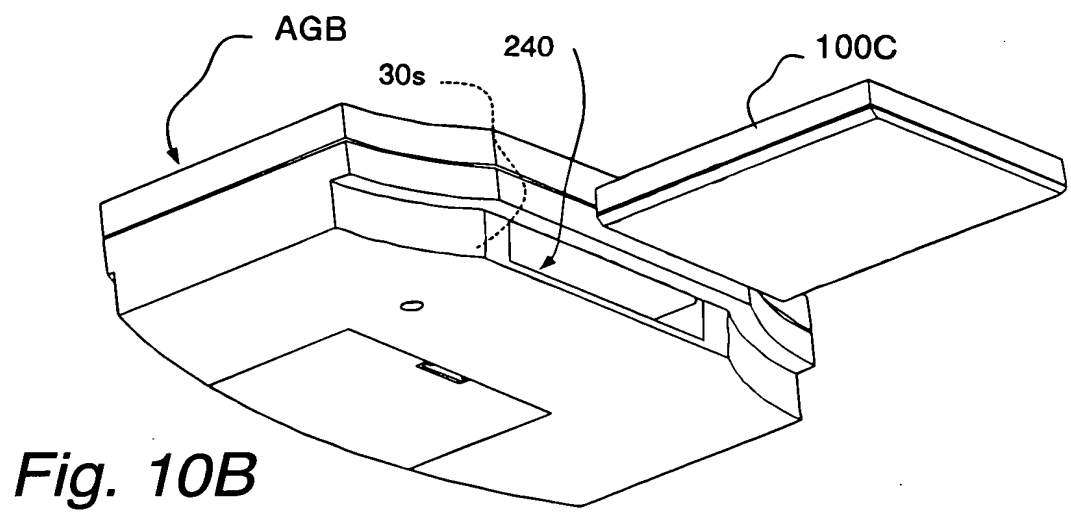
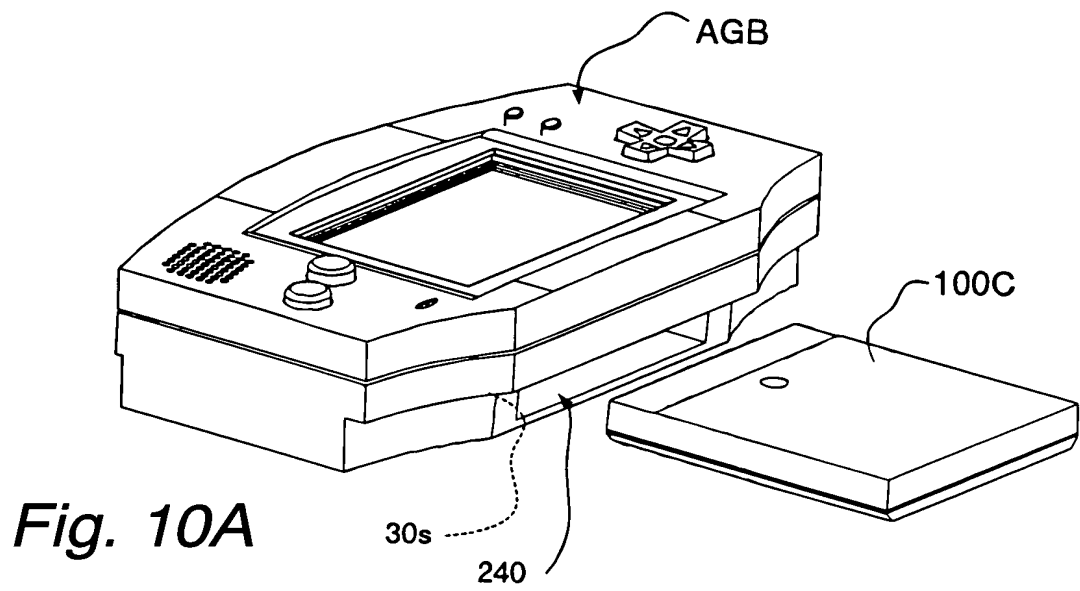


Fig. 8C





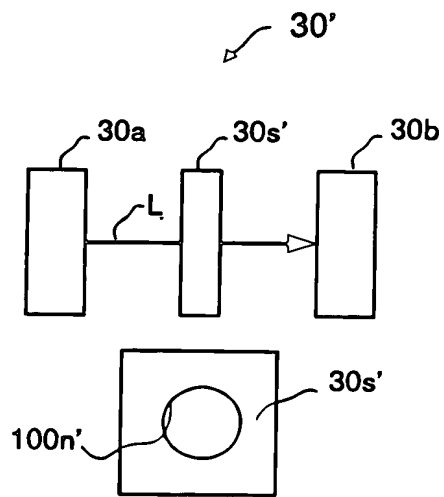


Fig. 11A

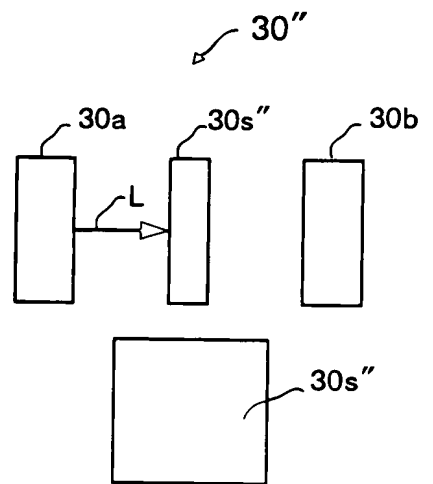


Fig. 11B

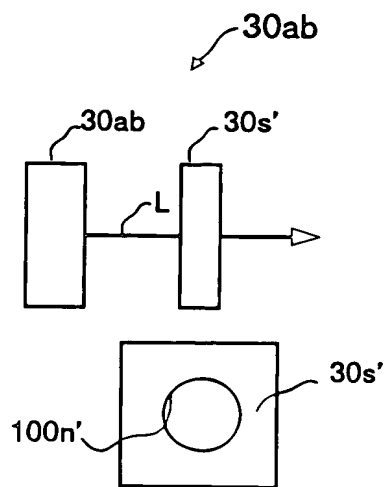


Fig. 11C

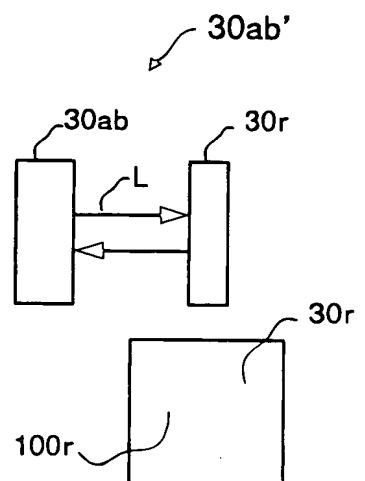


Fig. 11D

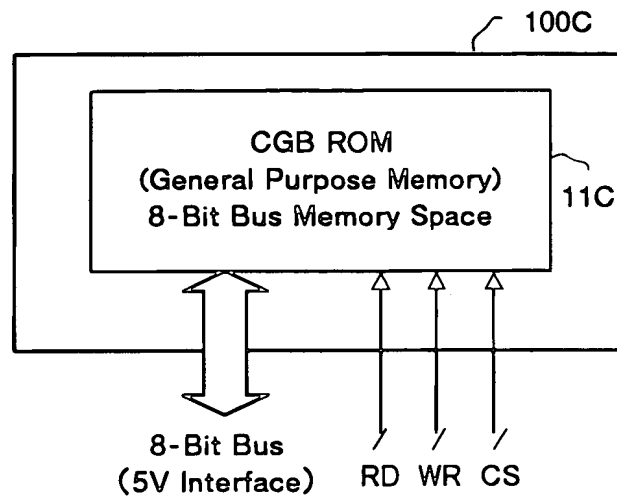


Fig. 12A

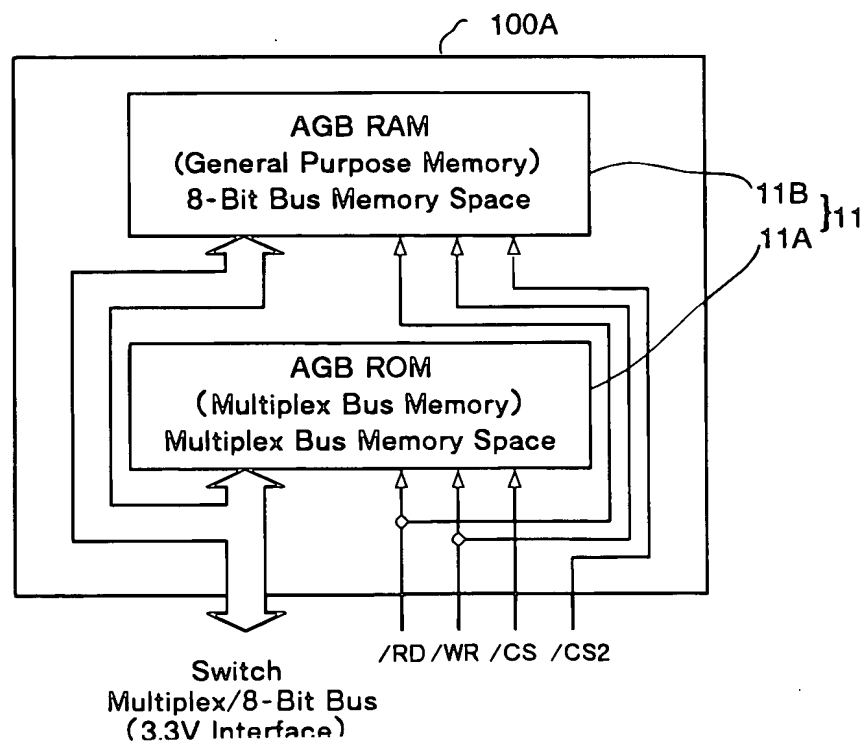


Fig. 12B

Fig. 14

NO	CGB	AGB ROM	AGB RAM	Remarks
1	VDD(5V)	VDD(3.3V)	VDD(3.3V)	Switch Voltage By Detection Switch
2	PHI	PHI	PHI	
3	/WR	/WR	/WR	
4	/RD	/RD	/RD	
5	/CS	/CS	/CS	Select ROM Chip
6	A0	A0/DO	A0	Address/Data Shared Terminal
7	A1	A1/D1	A1	Same As Above
8	A2	A2/D2	A2	Same As Above
9	A3	A3/D3	A3	Same As Above
10	A4	A4/D4	A4	Same As Above
11	A5	A5/D5	A5	Same As Above
12	A6	A6/D6	A6	Same As Above
13	A7	A7/D7	A7	Same As Above
14	A8	A8/D8	A8	Same As Above
15	A9	A9/D9	A9	Same As Above
16	A10	A10/D10	A10	Same As Above
17	A11	A11/D11	A11	Same As Above
18	A12	A12/D12	A12	Same As Above
19	A13	A13/D13	A13	Same As Above
20	A14	A14/D14	A14	Same As Above
21	A15	A15/D15	A15	Same As Above
22	D0	A16	D0	
23	D1	A17	D1	
24	D2	A18	D2	
25	D3	A19	D3	
26	D4	A20	D4	
27	D5	A21	D5	
28	D6	A22	D6	
29	D7	A23	D7	
30	/RES	/CS2	/CS2	Action Each Different In AGB and CGB Modes
31	Not Allowed to Use (VIN)	IREQ/ DREQ	IREQ/ DREQ	In CGB Mode, Ignore VIN Input
32	GND	GND	GND	

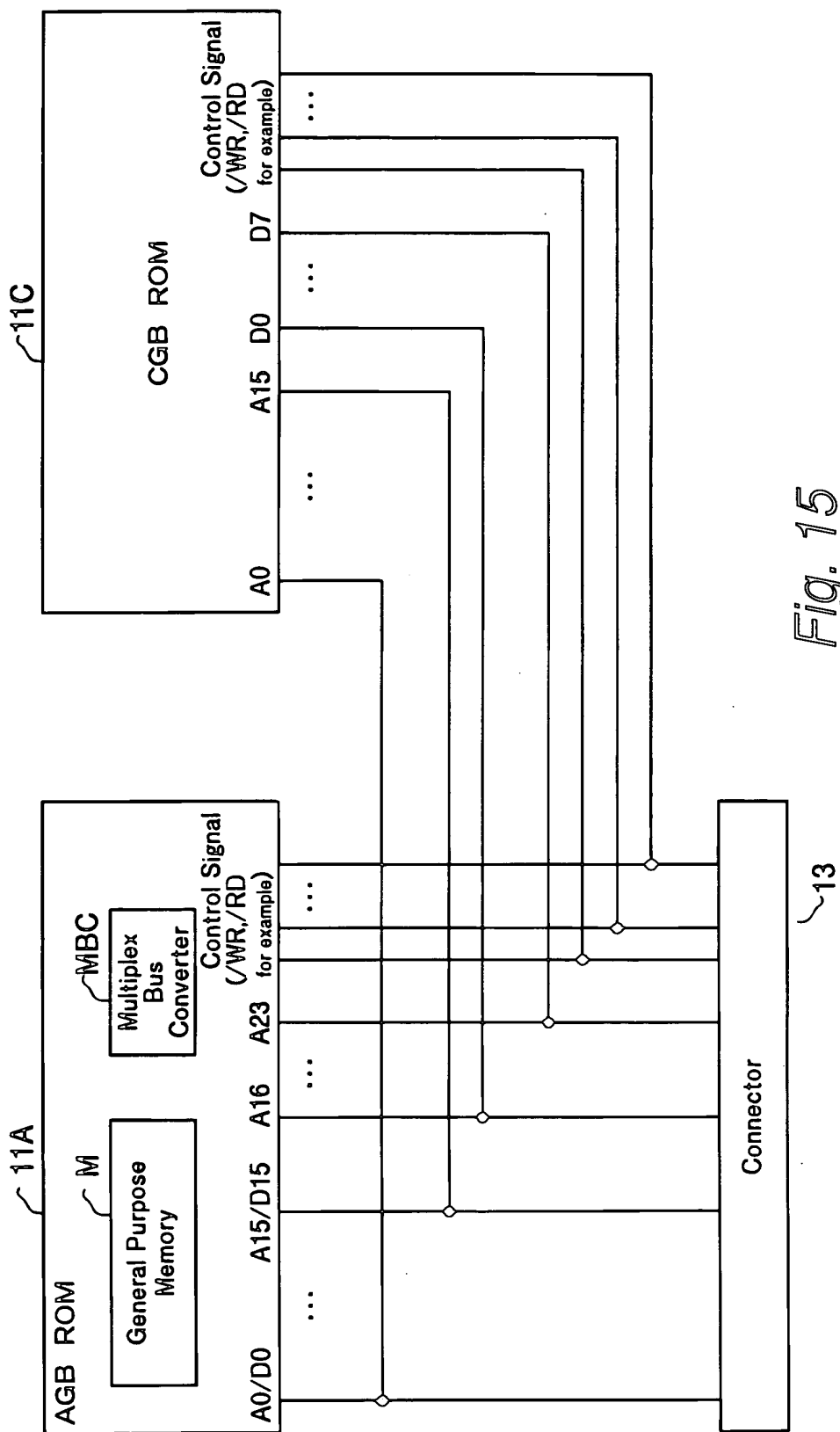


Fig. 15

Fig. 16A

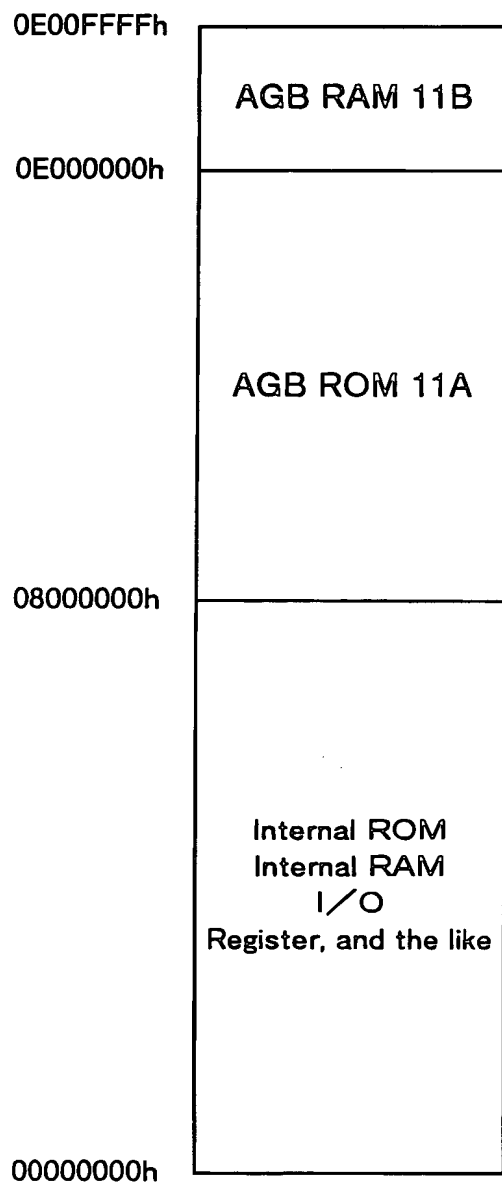


Fig. 16C

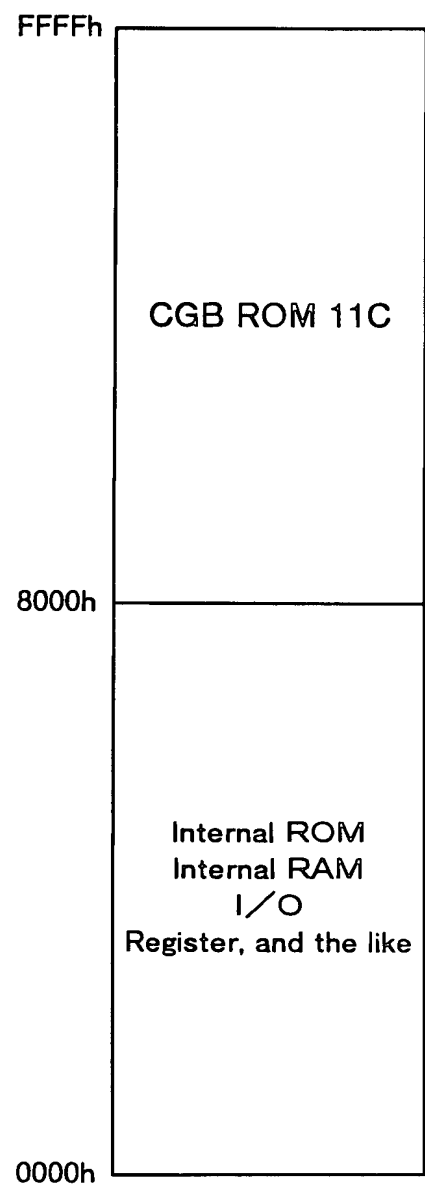


Fig. 16B

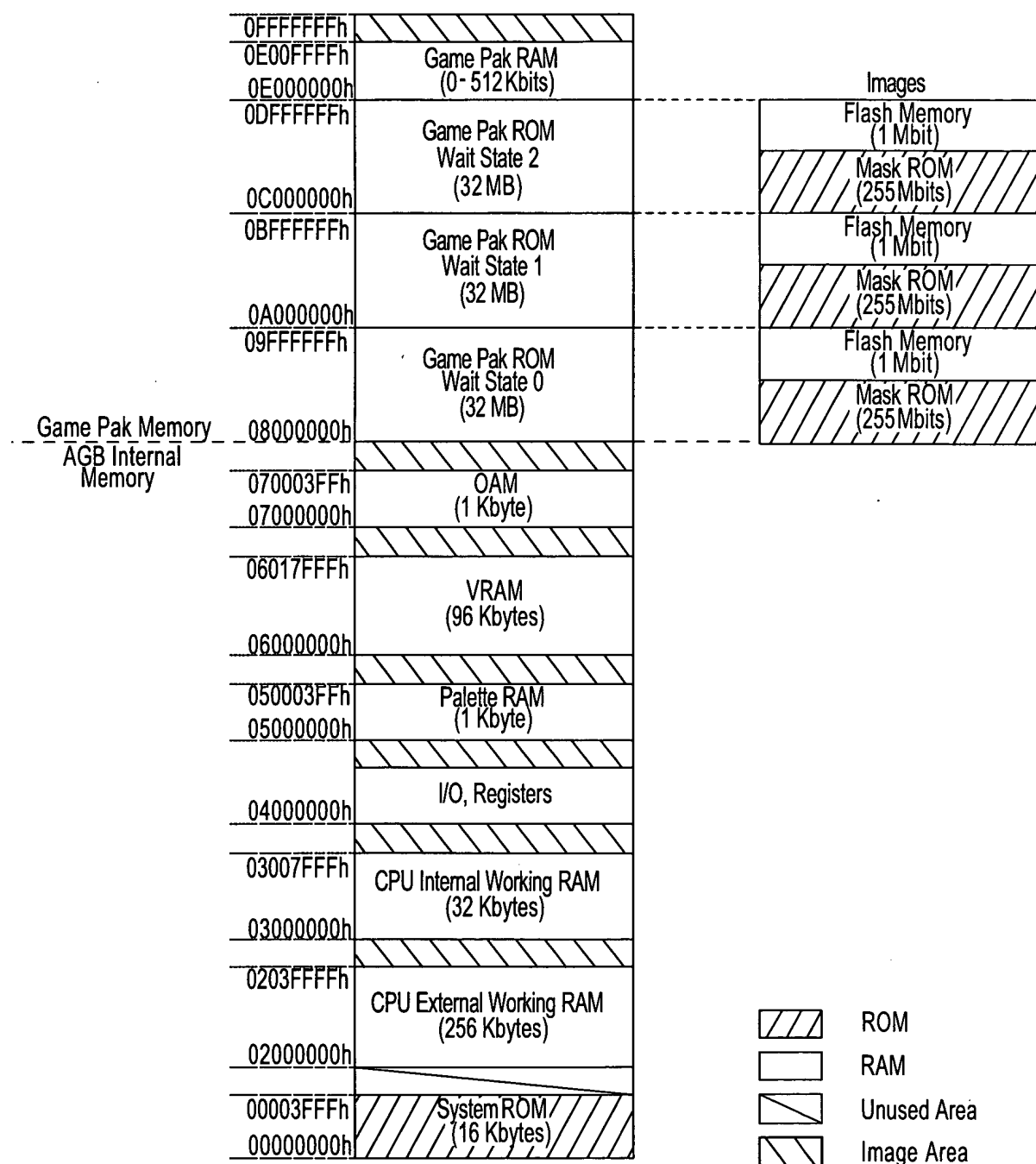
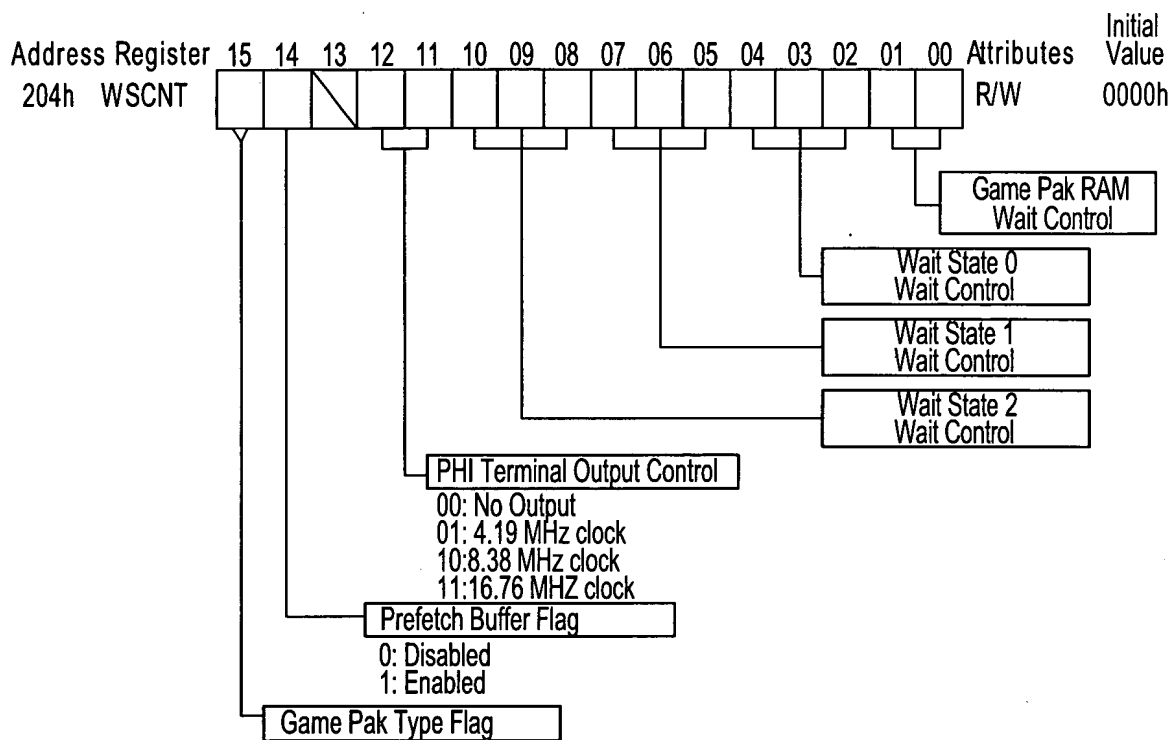


Fig. 17



AGB ROM11A Read Access

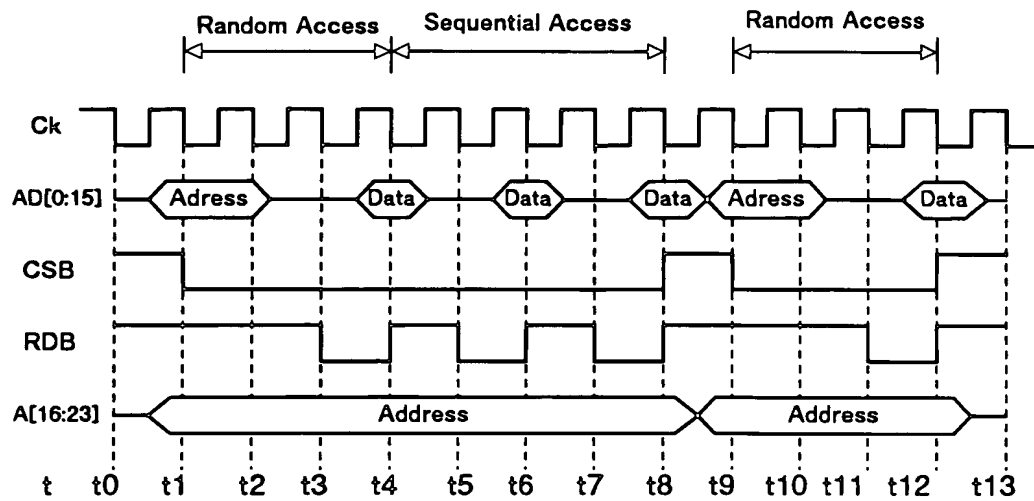


Fig. 18A

AGB RAM11B Write Access

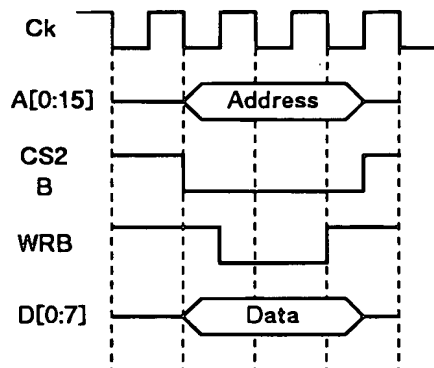


Fig. 18D

AGB RAM11B Read Access

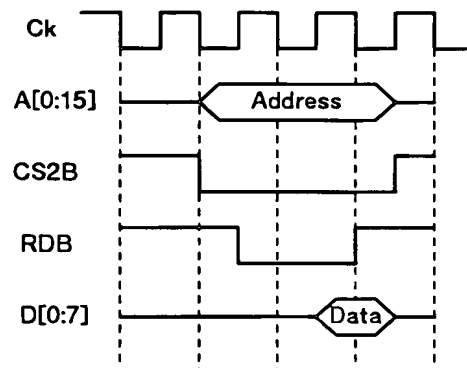


Fig. 18E

CGB ROM11C Read Access

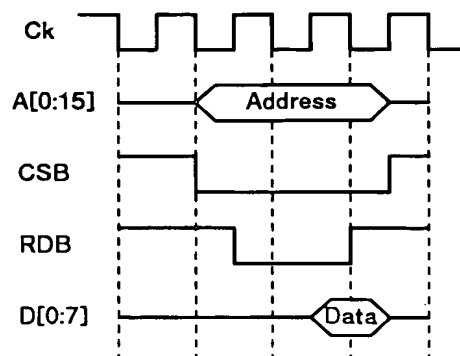


Fig. 18F

Fig. 18B

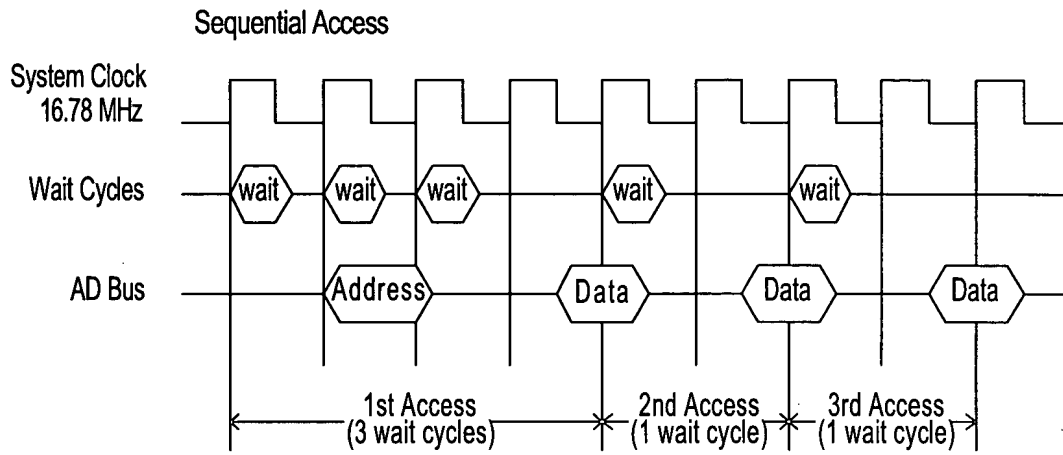
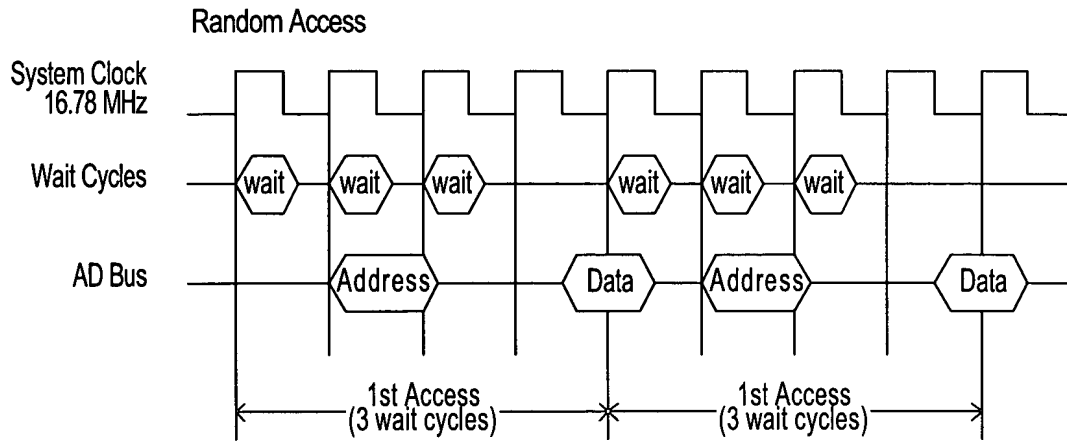


Fig. 18C



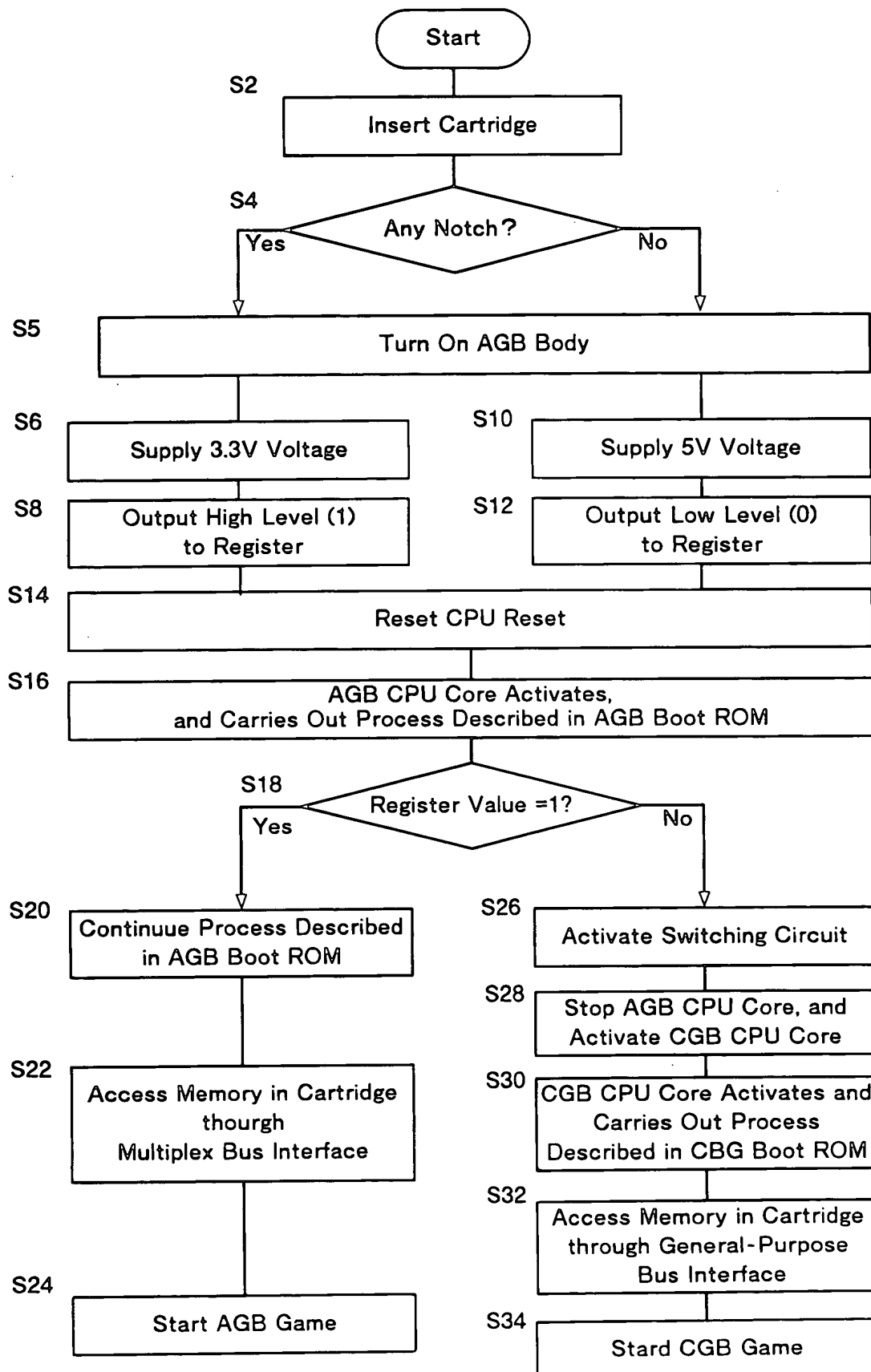


Fig. 20

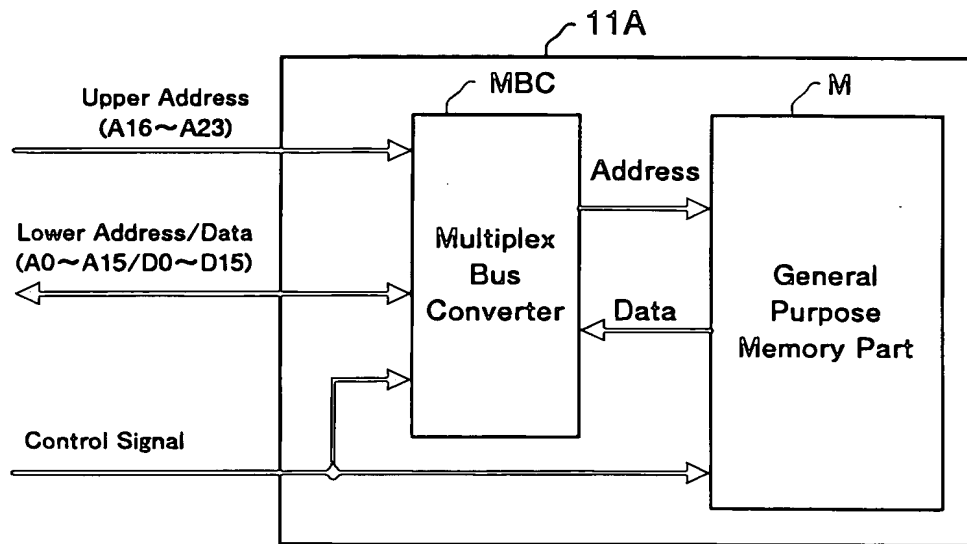


Fig. 21A

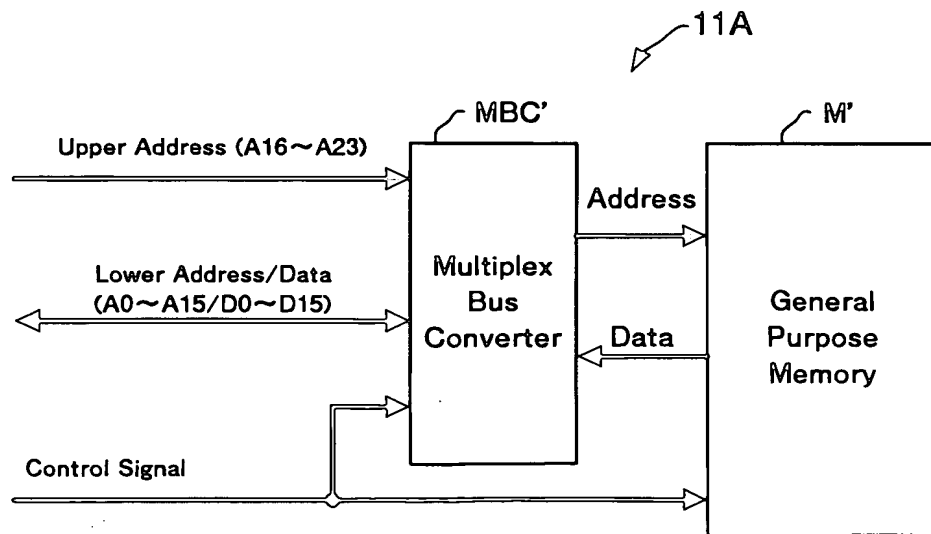


Fig. 21B

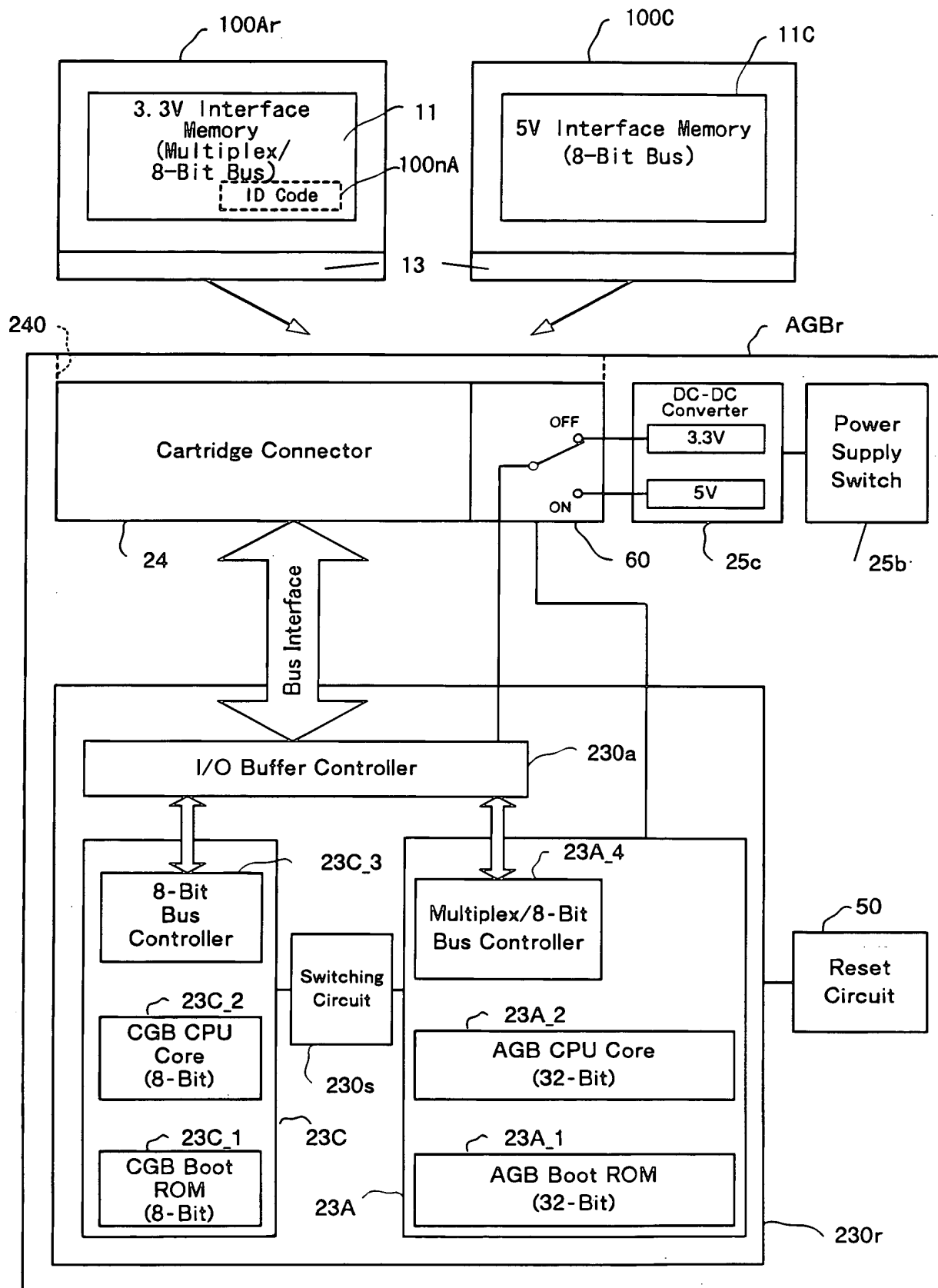


Fig. 22

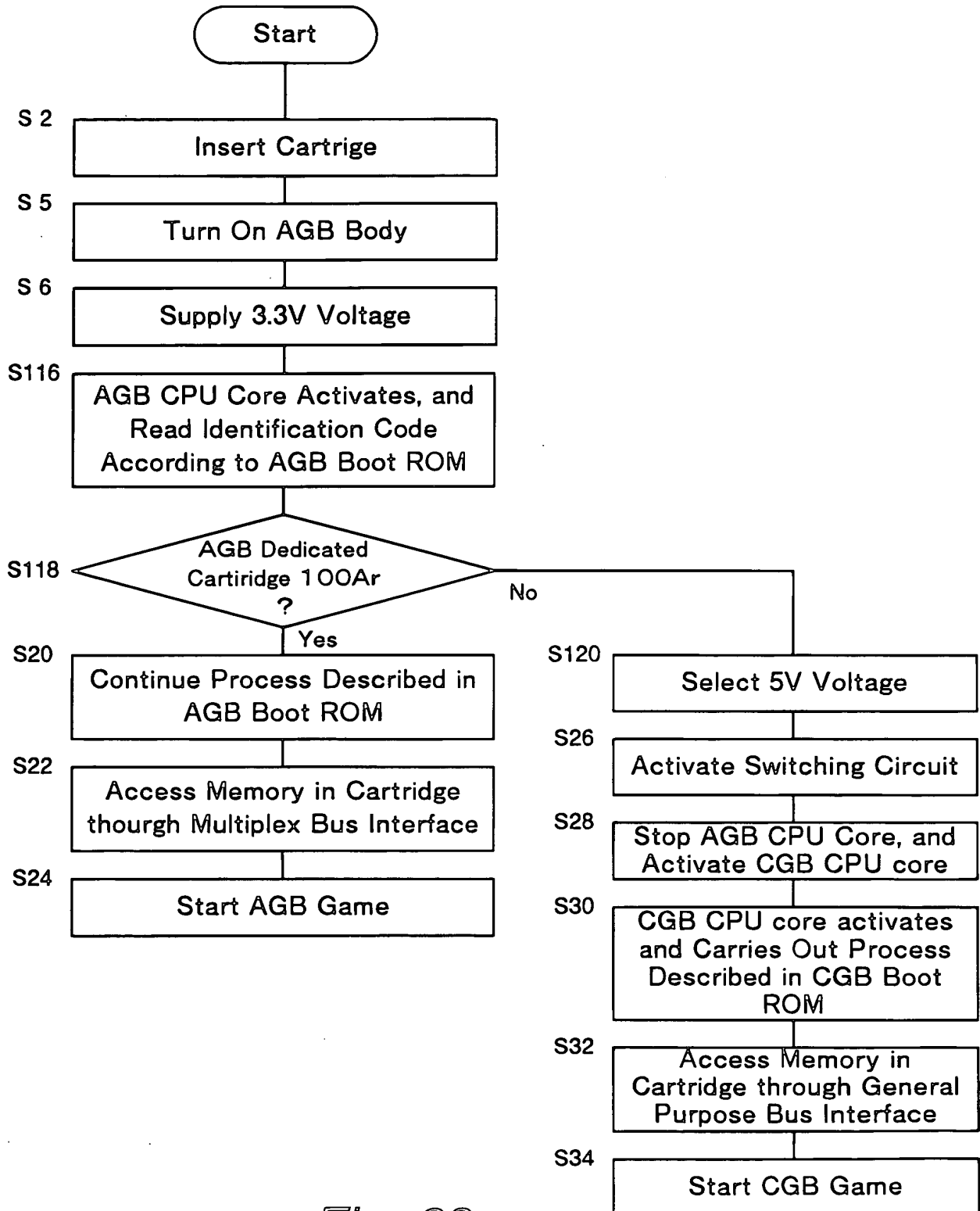


Fig. 23

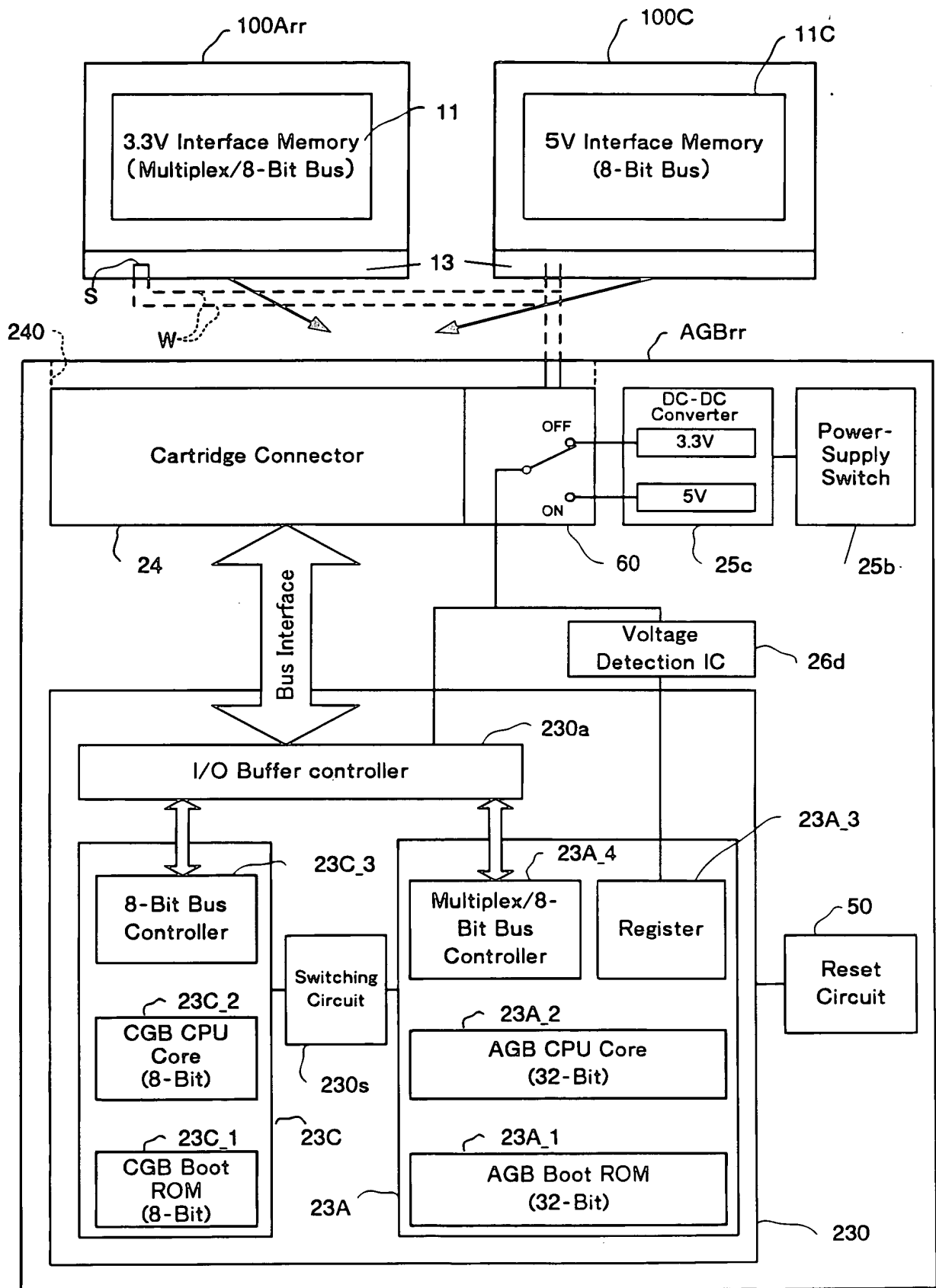


Fig. 24

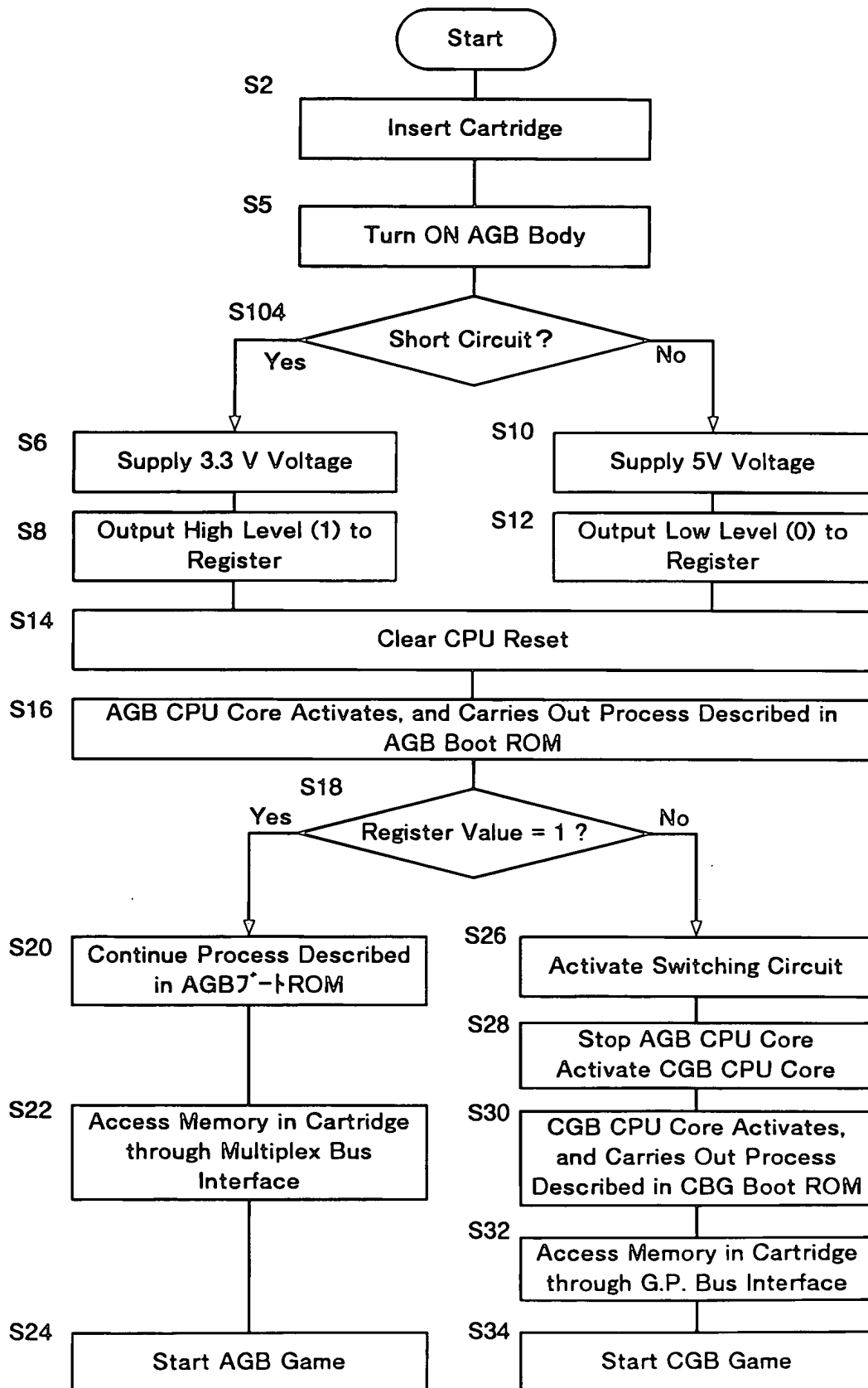


Fig. 25

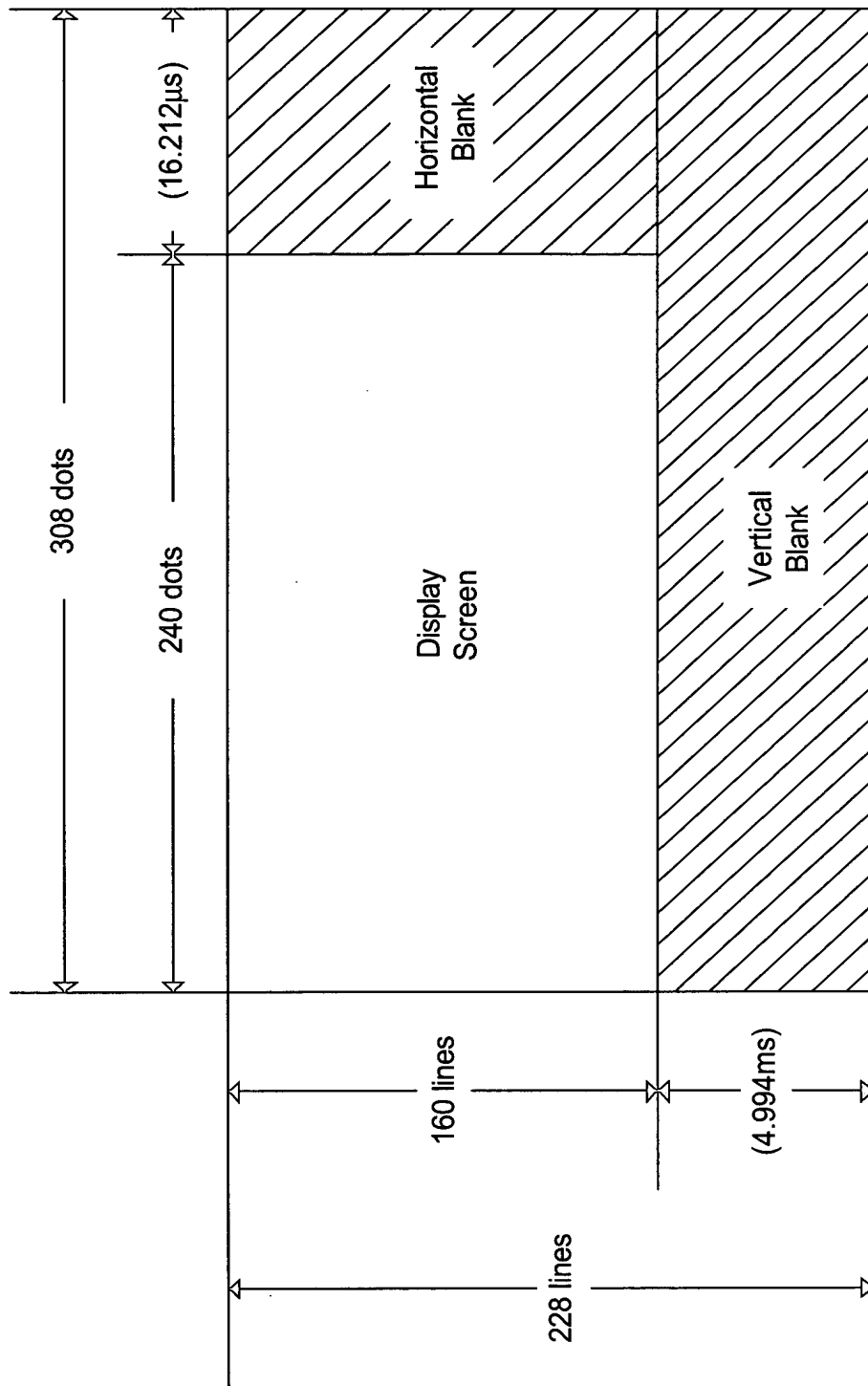


Fig. 26

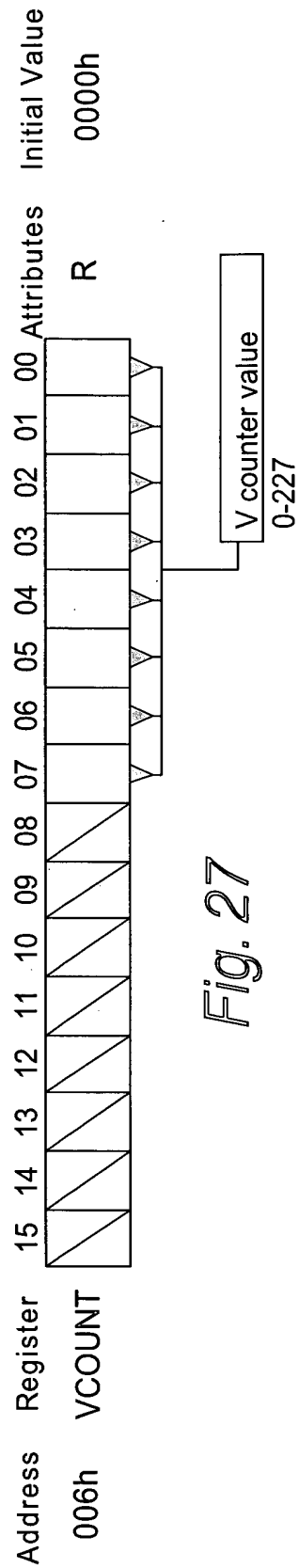


Fig. 27

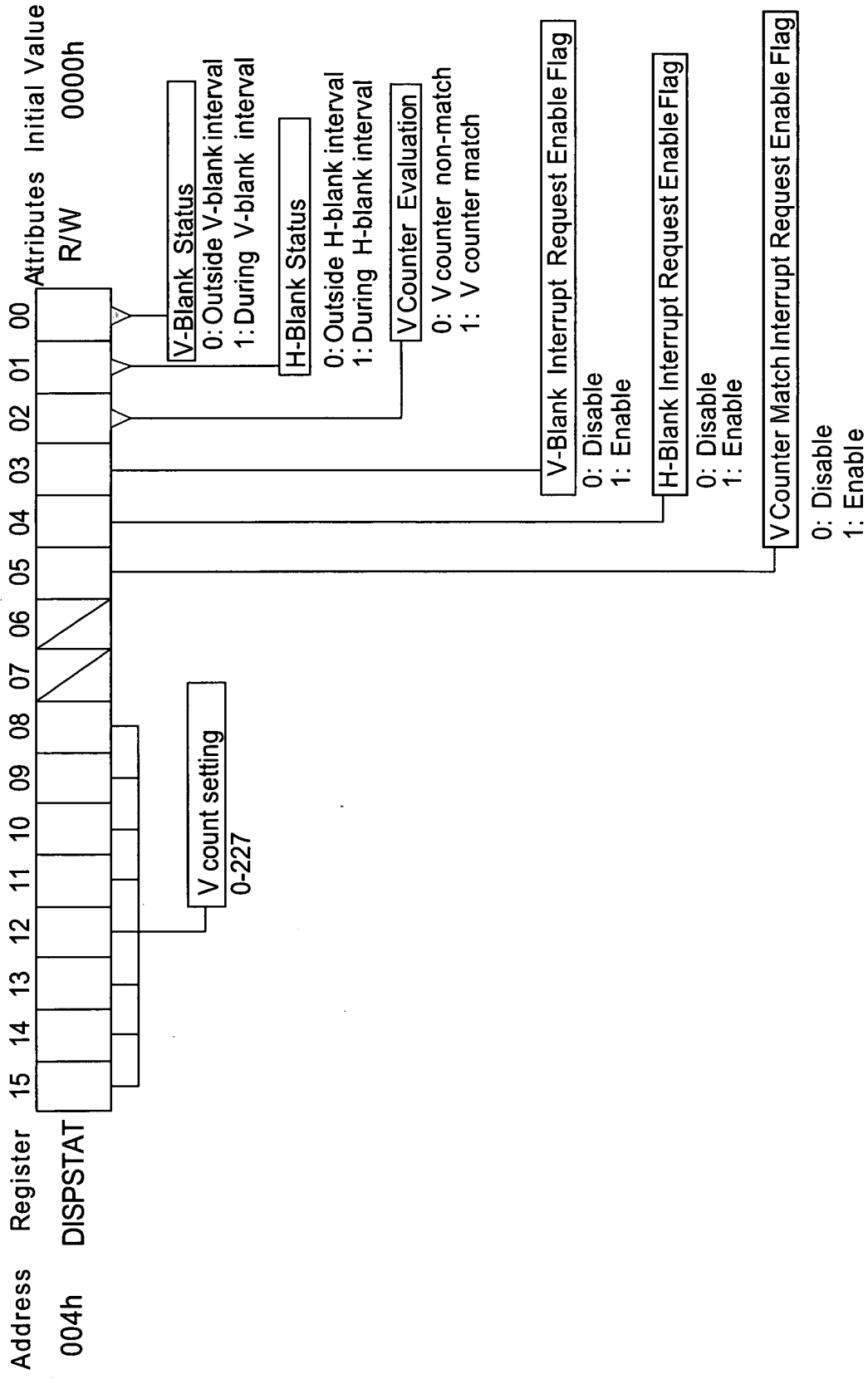


Fig. 28

Fig. 29

Fig. 30A

BG Mode	Character Format BG Screen			Number of Characters Specifiable	Number of Colors/ Palettes	Features					
	Rotation/ scaling	No. of Screens	Size			*1	*2	*3	*4	*5	*6
0	No	4	256 x 256 to 512 x 512	1024	16/16 256/1	O	O	O	O	O	O
1	No	2	256 x 256 to 512 x 512	1024	16/16 256/1	O	O	O	O	O	O
	Yes	1	128 x 128 to 1024 x 1024	256	256/1	O	X	O	O	O	O
2	Yes	2	128 x 128 to 1024 x 1024	256	256/1	O	X	O	O	O	O

*1 HV Scroll (individual screens)
*2 HV Flip (individual characters)
*3 Mosaic (16 levels)

*4 Semi-transparent (16 levels)
*5 Fade-in/Fade-out
*6 Screen priority specification (2 bits)

Fig. 30B

BG Mode	Bitmap Format BG Screen			Frame Memory	No. of Colors	Features					
	Rotation/ Scaling	No. of Screens	Size			*1	*2	*3	*4	*5	*6
3	Yes	1	240 x 160	1	32,768	O	X	O	O	O	O
4	Yes	1	240 x 160	2	256	O	X	O	O	O	O
5	Yes	1	160 x 128	2	32,768	O	X	O	O	O	O

*1 HV Scroll (individual screens)
*2 HV Flip (individual characters)
*3 Mosaic (16 levels)

*4 Semi-transparent (16 levels)
*5 Fade-in/Fade-out
*6 Screen priority specification (2 bits)

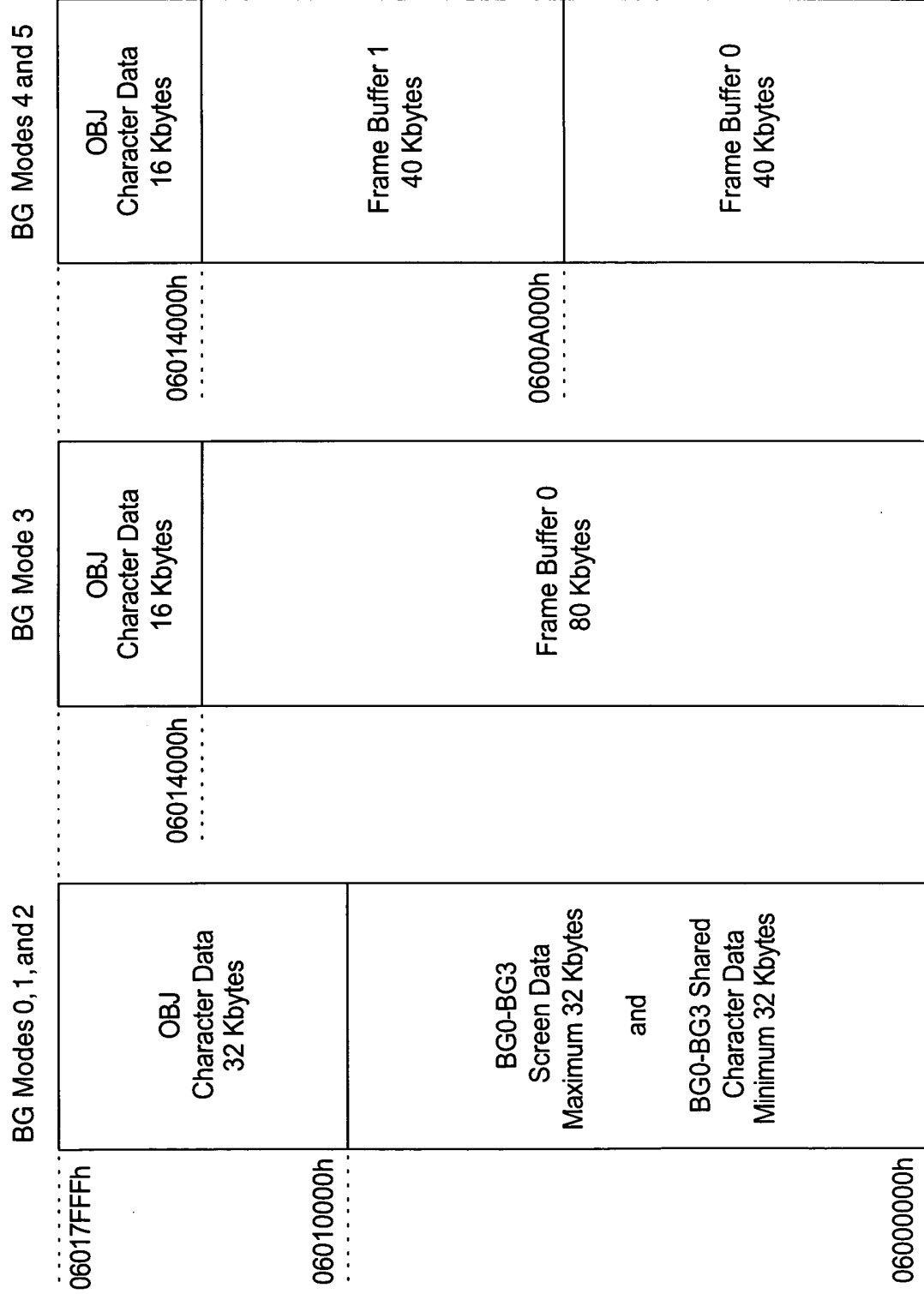


Fig. 31

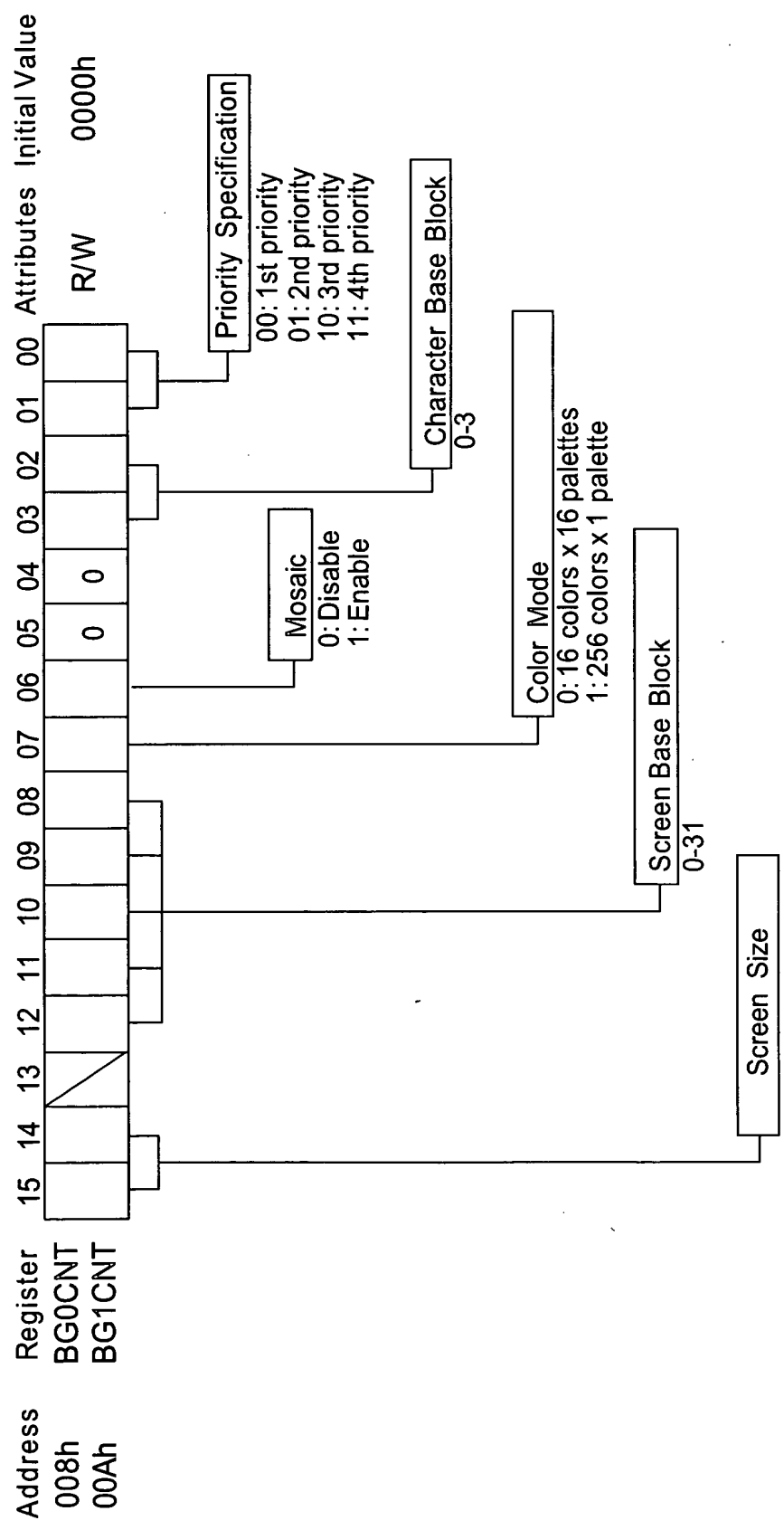


Fig. 32A

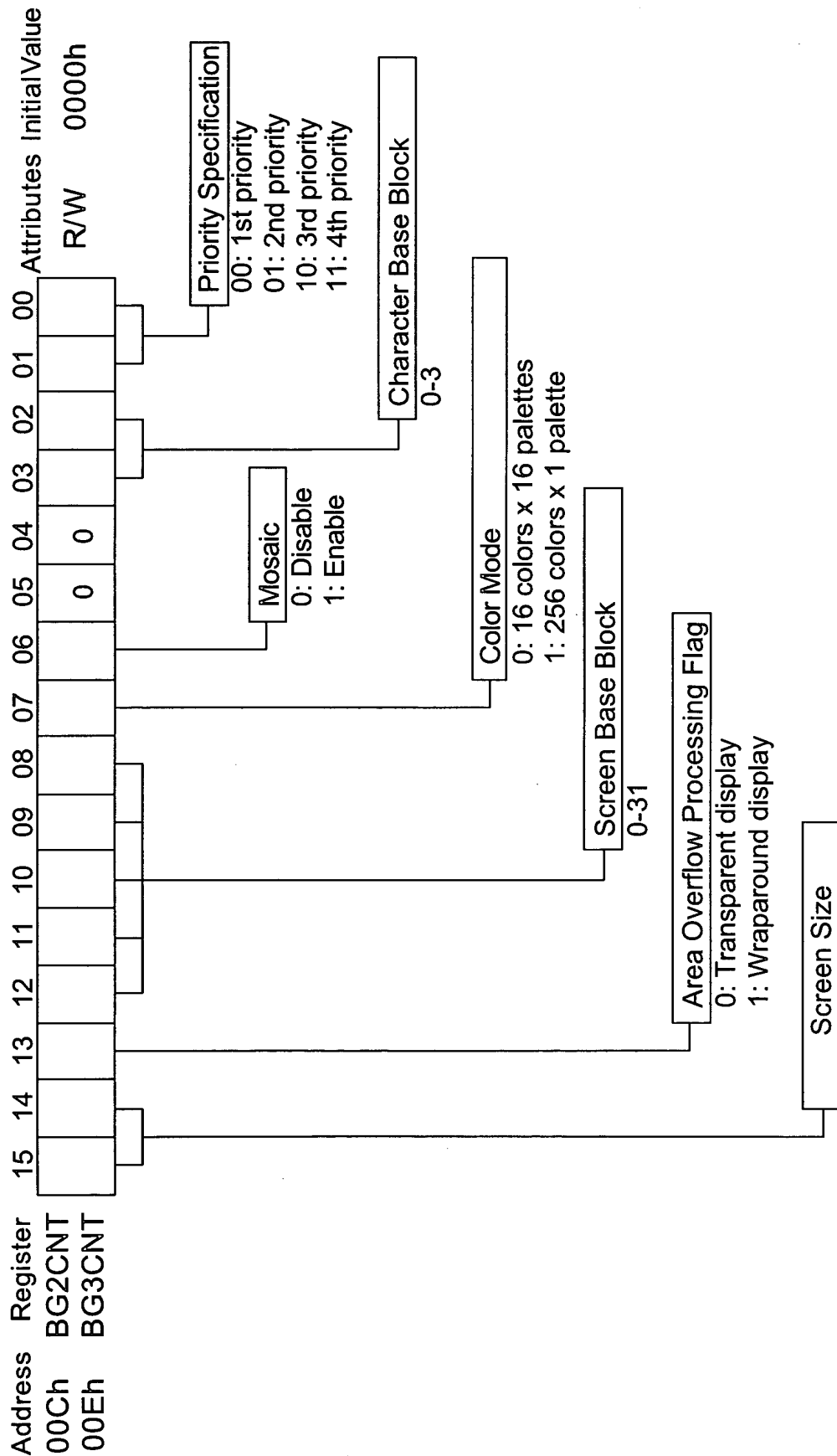


Fig. 32B

[d15,d14]=[0,0] Virtual screen size: 256 x 256

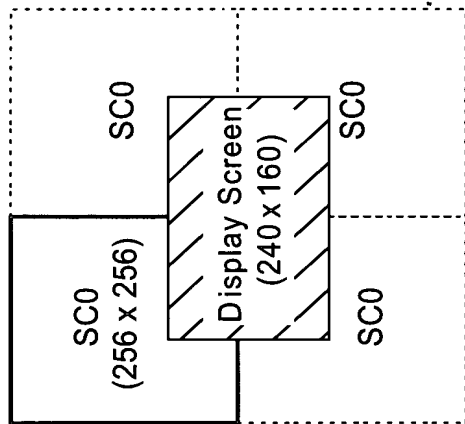


Fig. 33A

[d15,d14]=[0,1] Virtual Screen size: 512 x 256

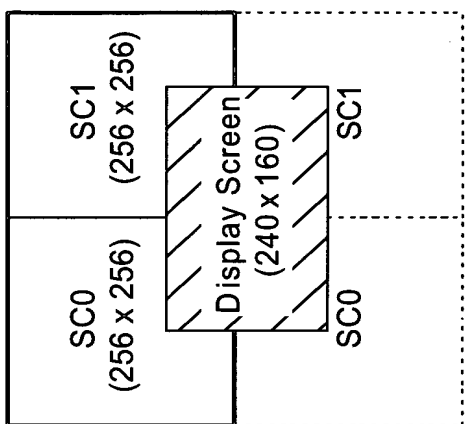


Fig. 33B

[d15,d14]=[1,0] Virtual screen size: 256 x 512

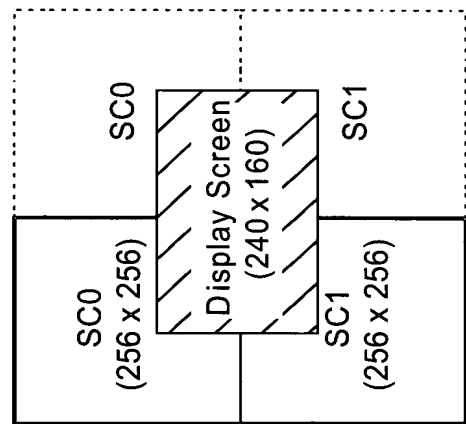


Fig. 33C

[d15,d14]=[1,1] Virtual screen size: 512 x 512

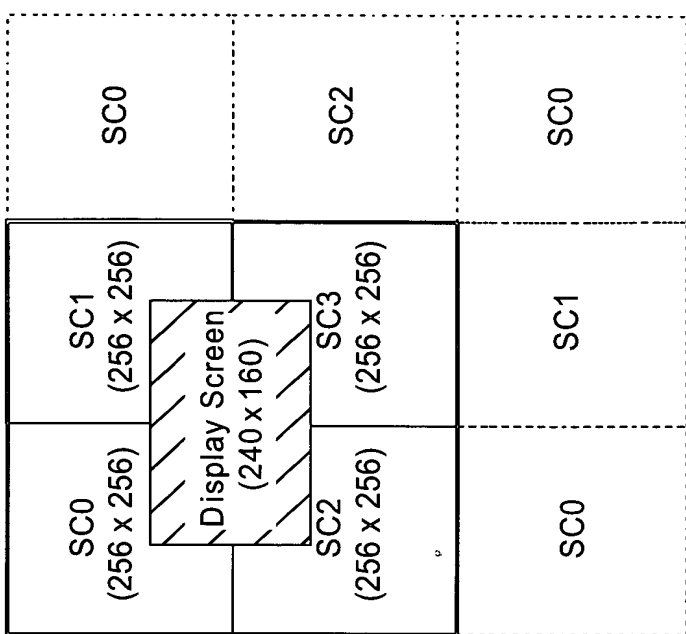


Fig. 33D

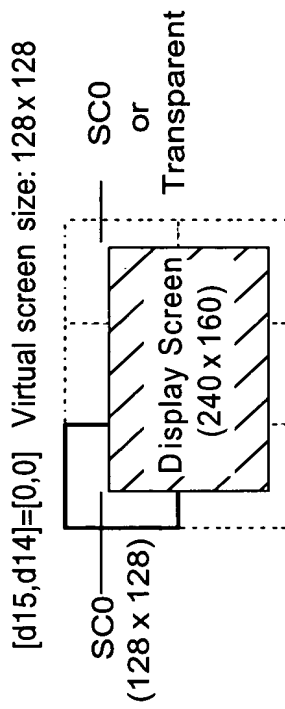


Fig. 34A

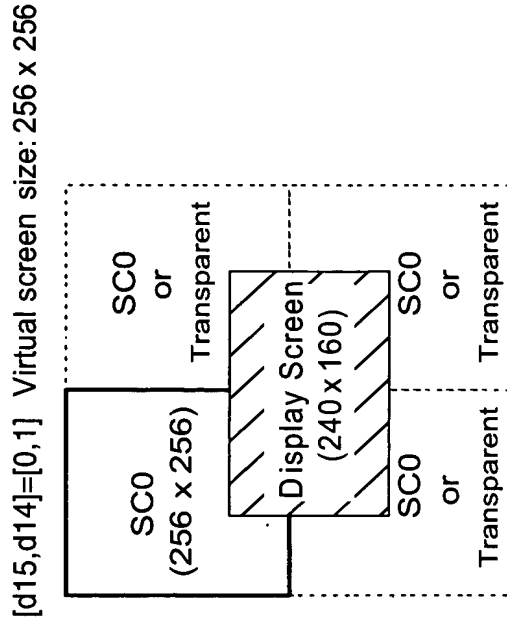


Fig. 34B

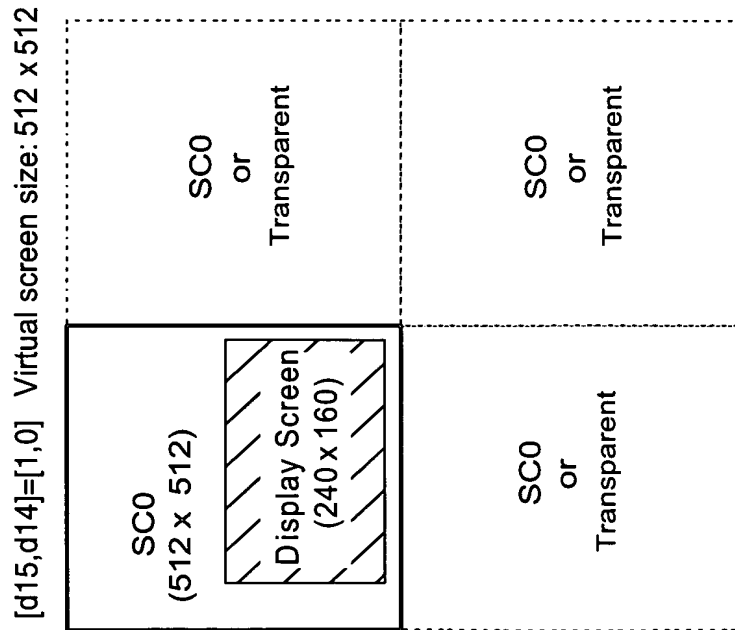


Fig. 34C

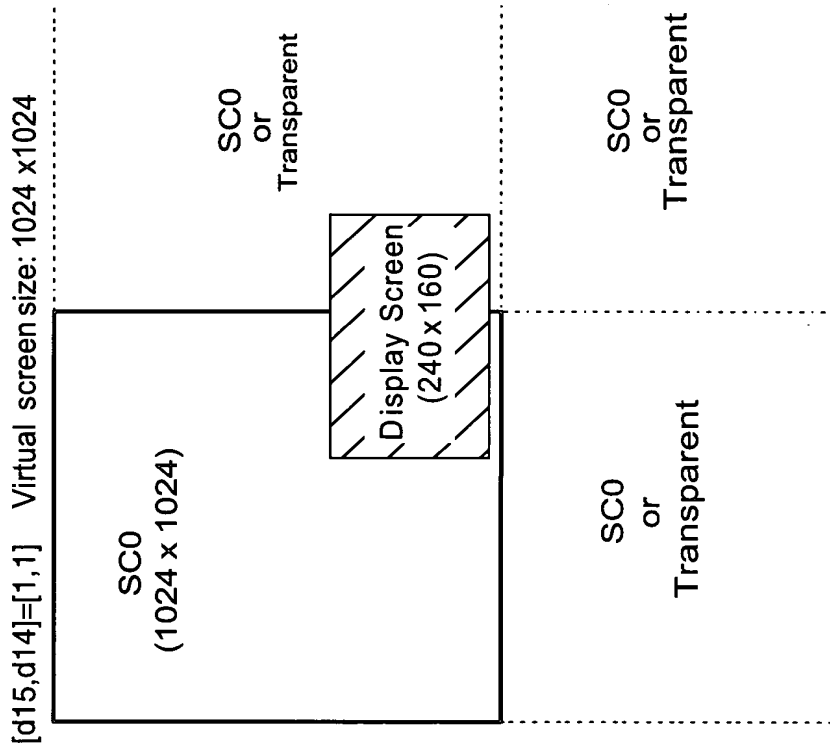


Fig. 34D

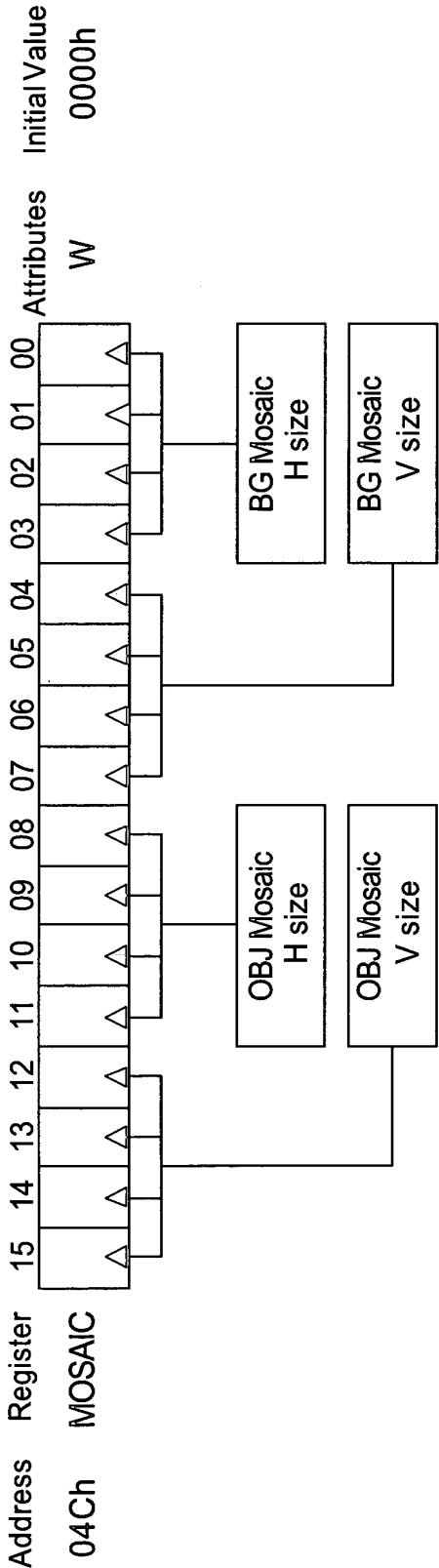


Fig. 35

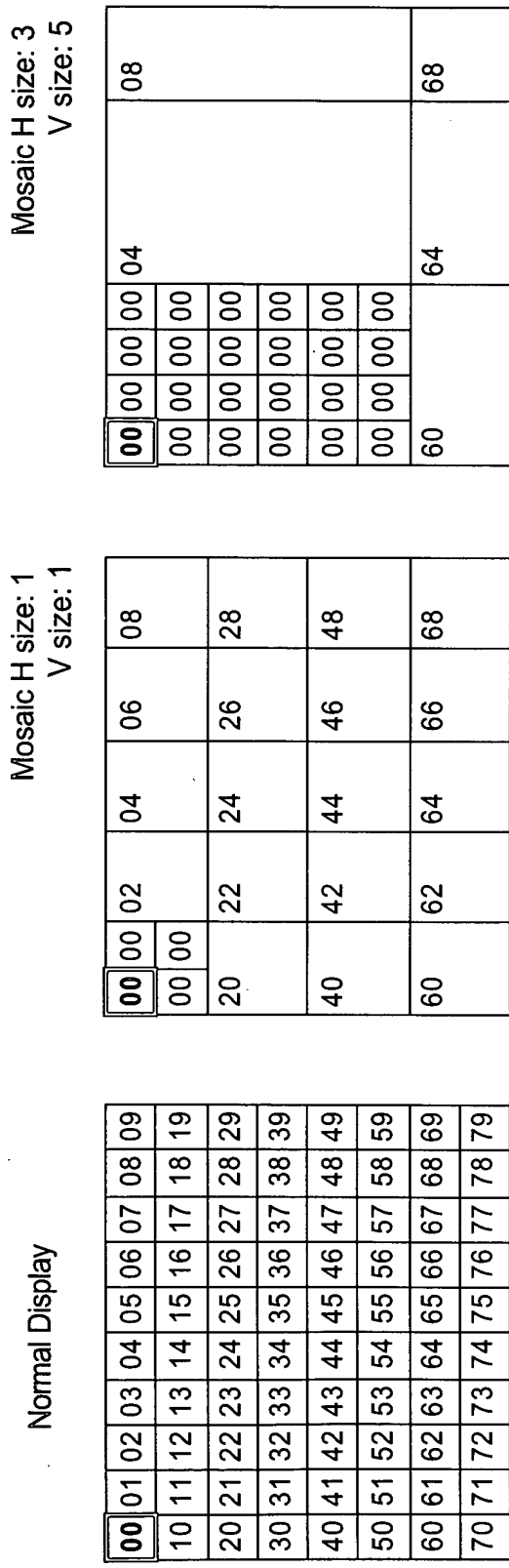


Fig. 36A

Fig. 36B

Fig. 36C

**BG Character Data
Base Block**

OBJ Character Data 32 Kbytes
Base Block 3
Base Block 2
Base Block 1
Base Block 0

**BG Screen Data
Base Block**

OBJ Character Data 32 Kbytes
Base Block 31
Base Block 30
Base Block 29
Base Block 28
Base Block 27
Base Block 26
Base Block 25
Base Block 24
Base Block 23
Base Block 22
Base Block 21
Base Block 20
Base Block 19
Base Block 18
Base Block 17
Base Block 16
Base Block 15
Base Block 14
Base Block 13
Base Block 12
Base Block 11
Base Block 10
Base Block 09
Base Block 08
Base Block 07
Base Block 06
Base Block 05
Base Block 04
Base Block 03
Base Block 02
Base Block 01
Base Block 00

10000h

C000h

8000h

4000h

0000h

Fig. 37

16 Colors x 16 Palettes

4 bits of data
per dot
(Specifies 1 of 16
colors)

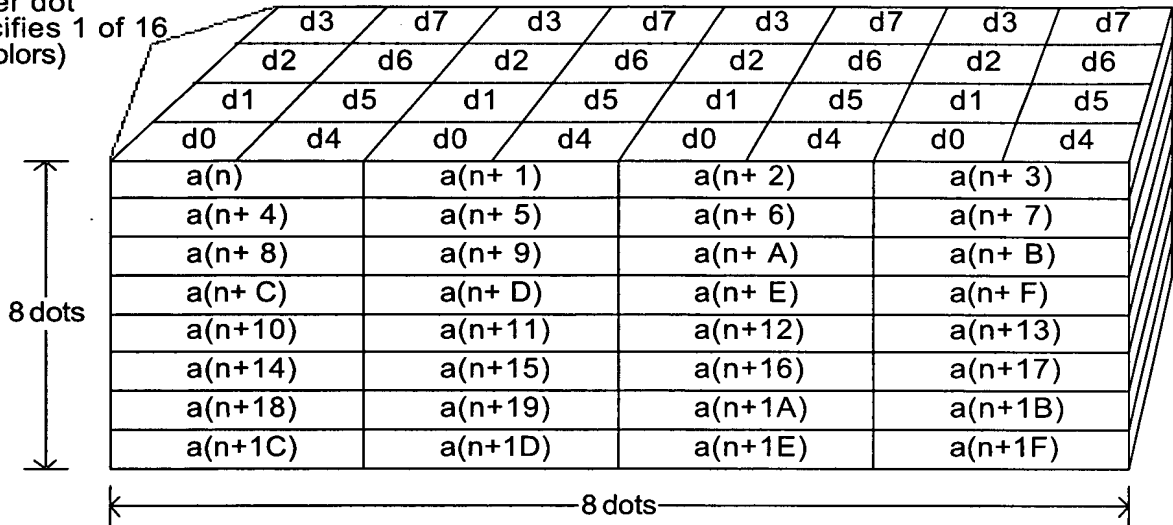


Fig. 38A

256 Colors x 1 Palettes

8 bits of data per dot
(Specifies 1 of 256
colors)

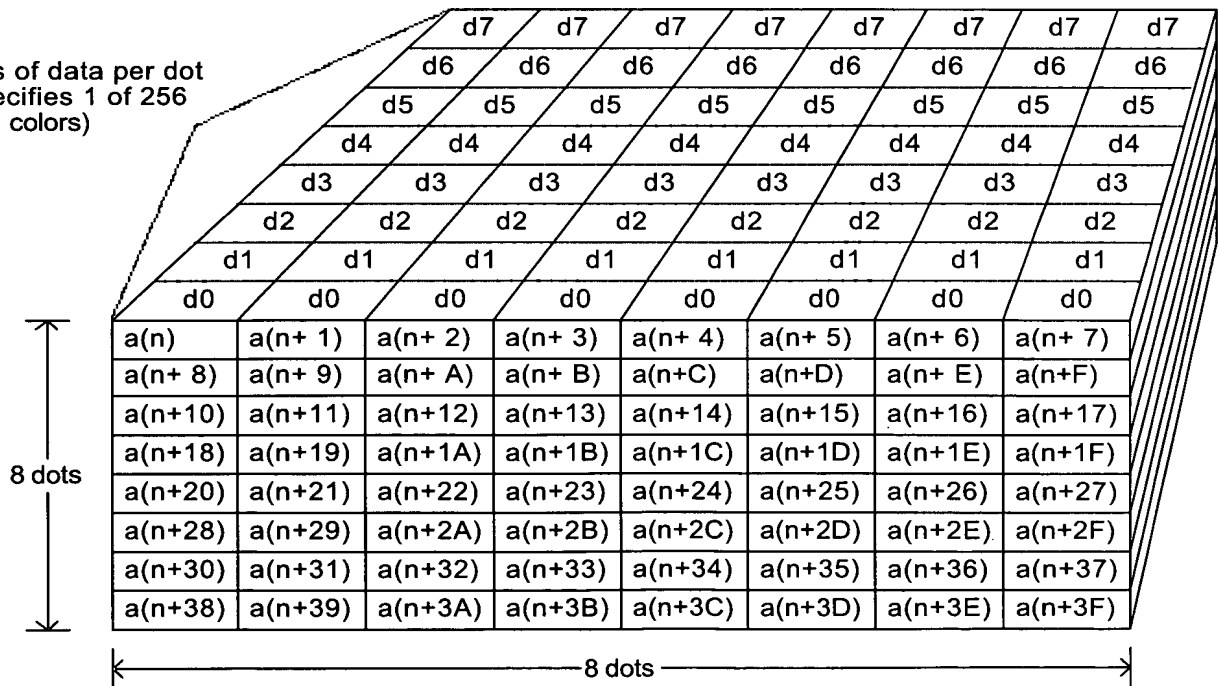


Fig. 38B

Text BG screen data format

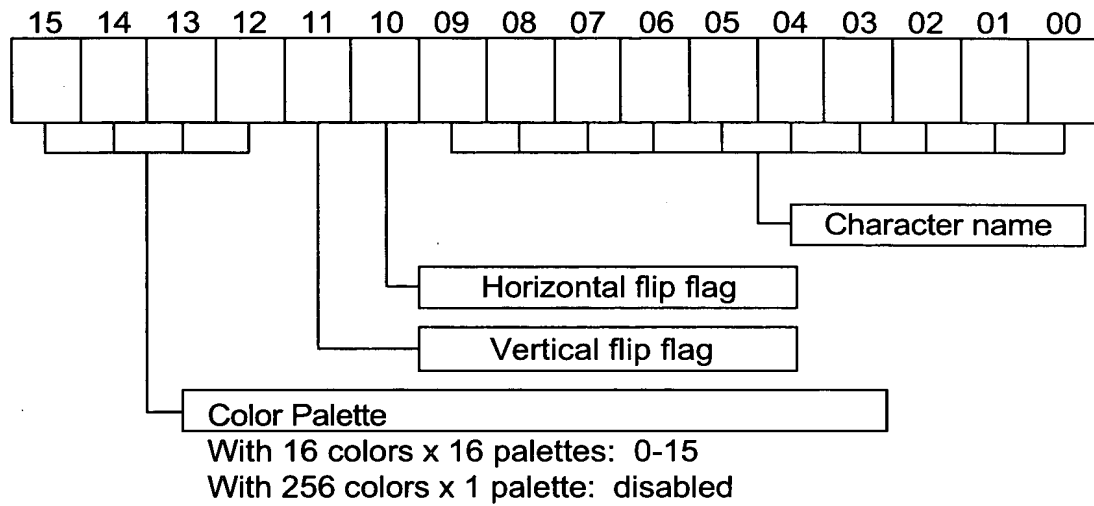


Fig. 39A

Rotation/scaling BG screen data format

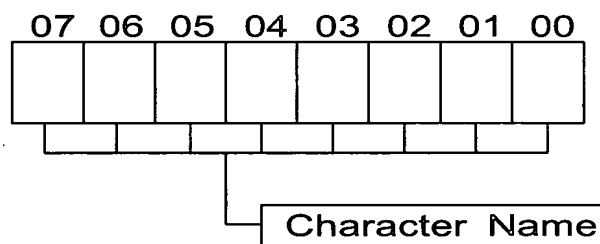
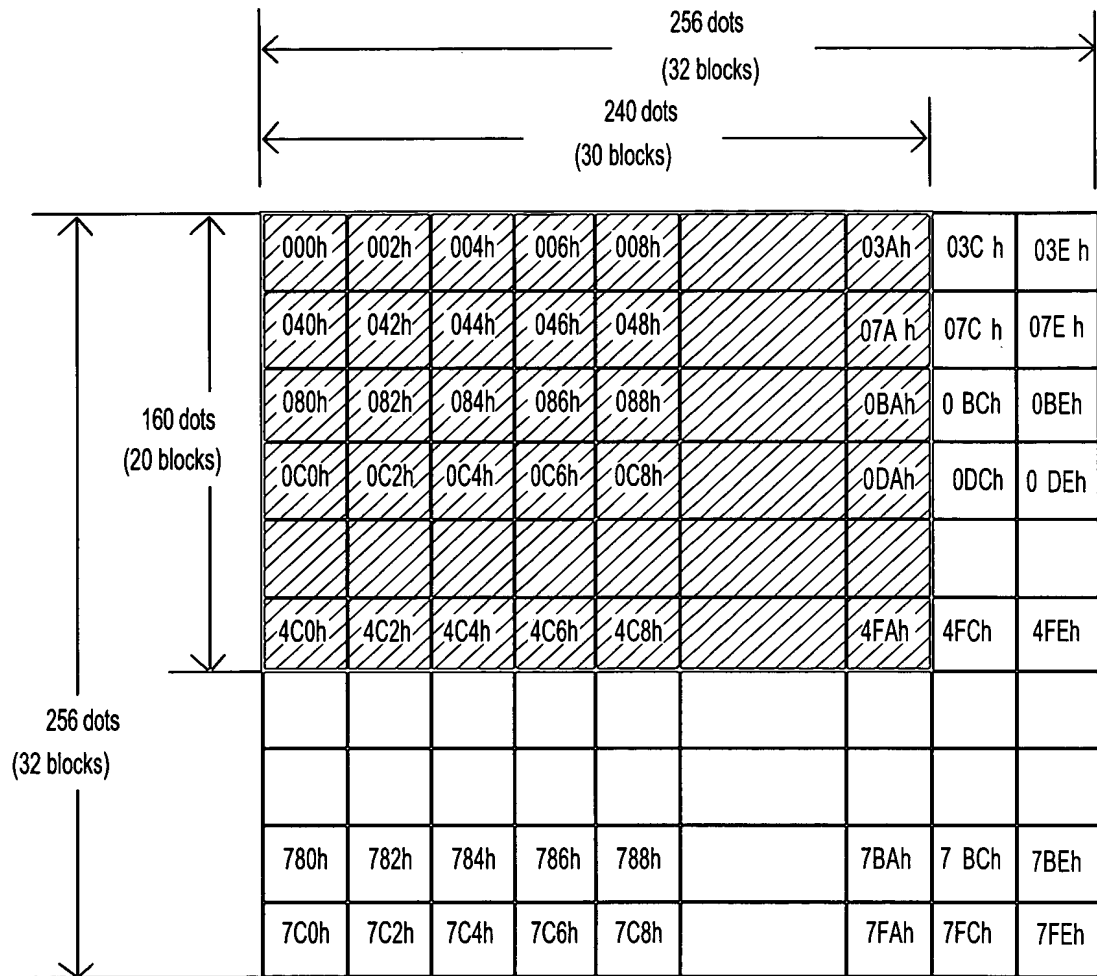
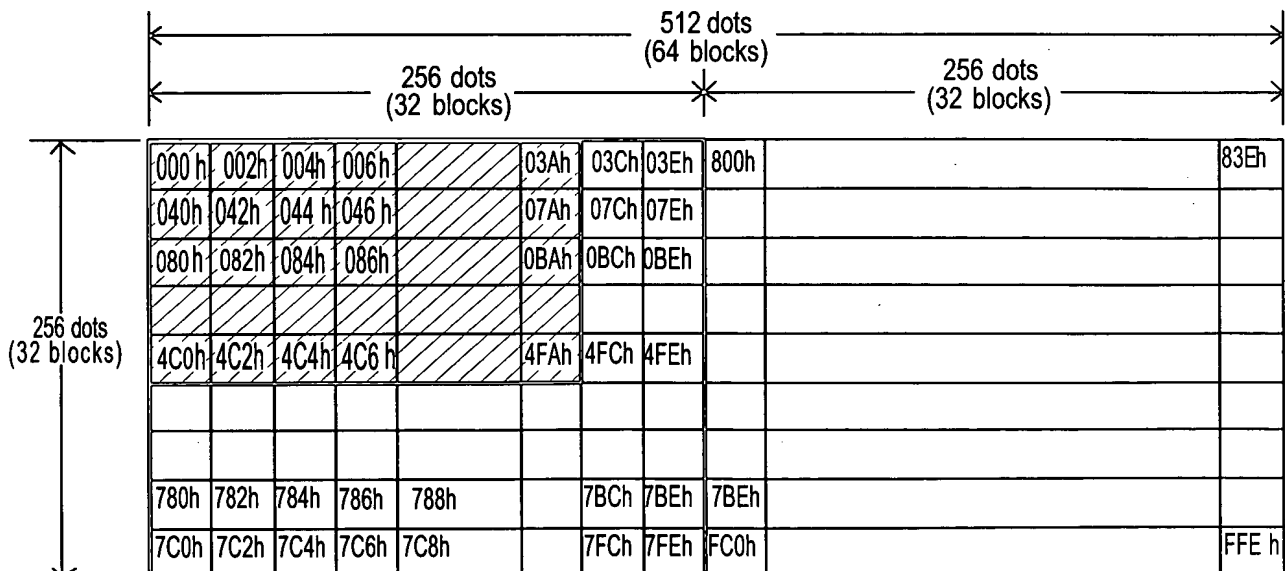


Fig. 39B



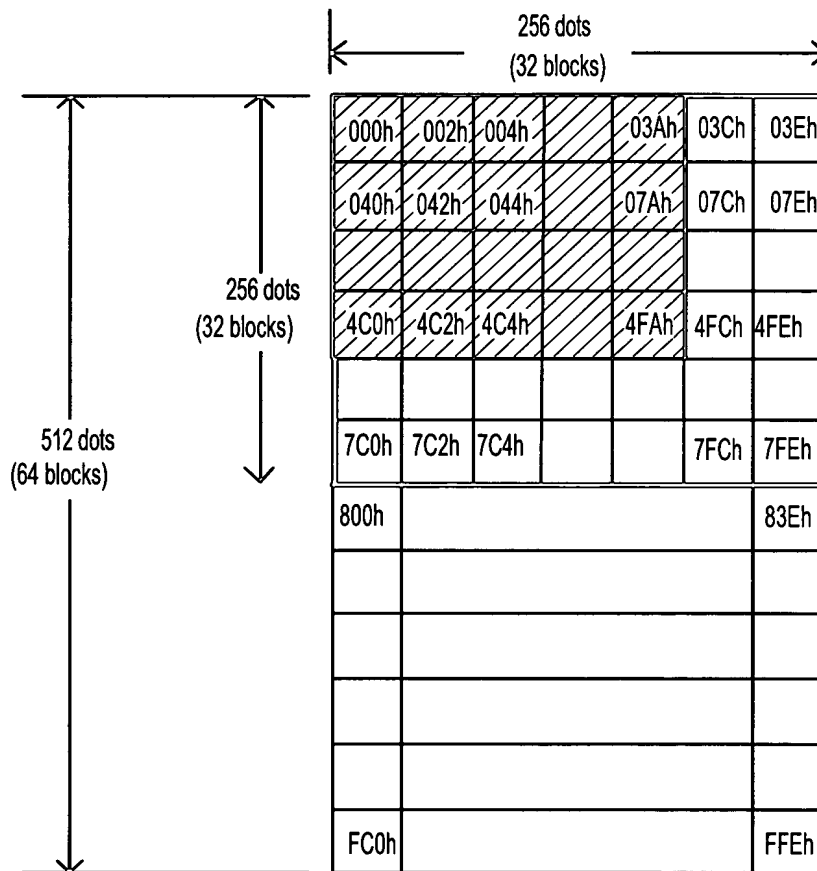
■ LCD Display Area

Fig. 40A



■ LCD Display Area

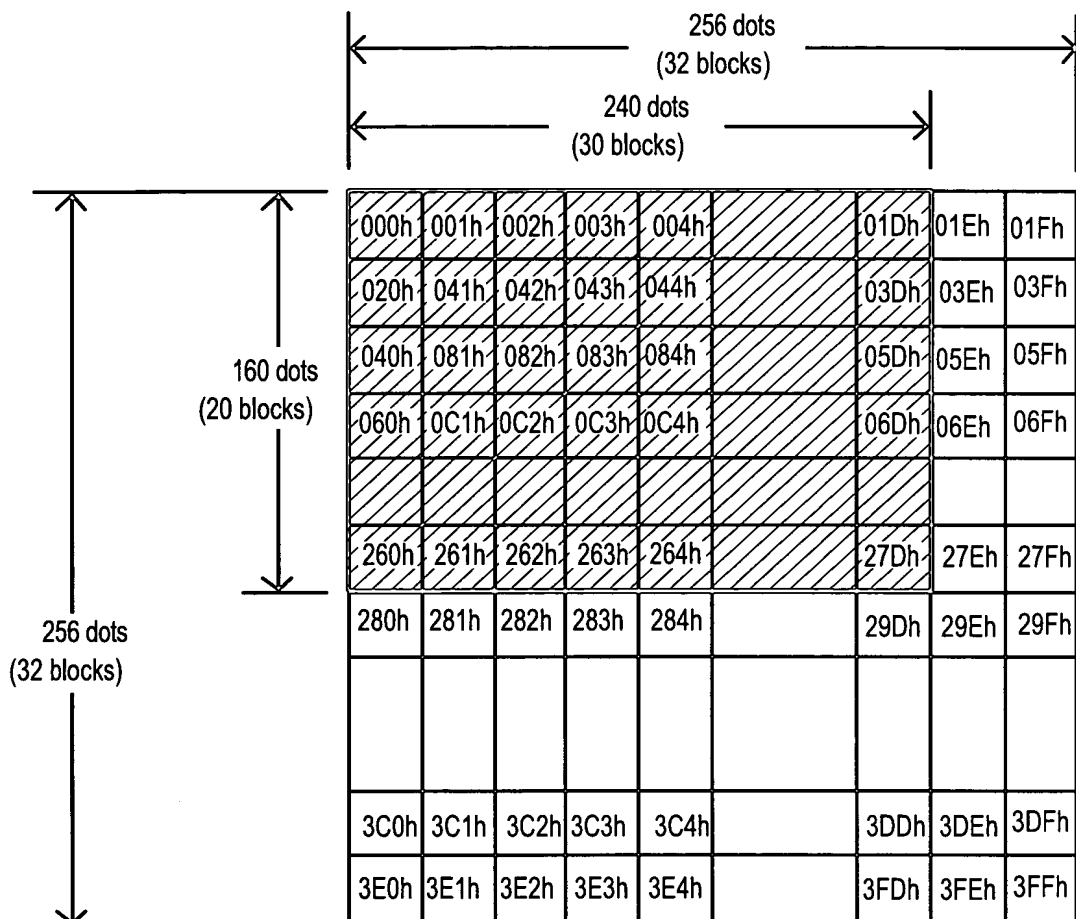
Fig. 40B



■ LCD Display Area

Fig. 40C

0000h 0001h 0002h 0003h 0004h



■ LCD Display Area

Fig. 41B

00000000 00000000

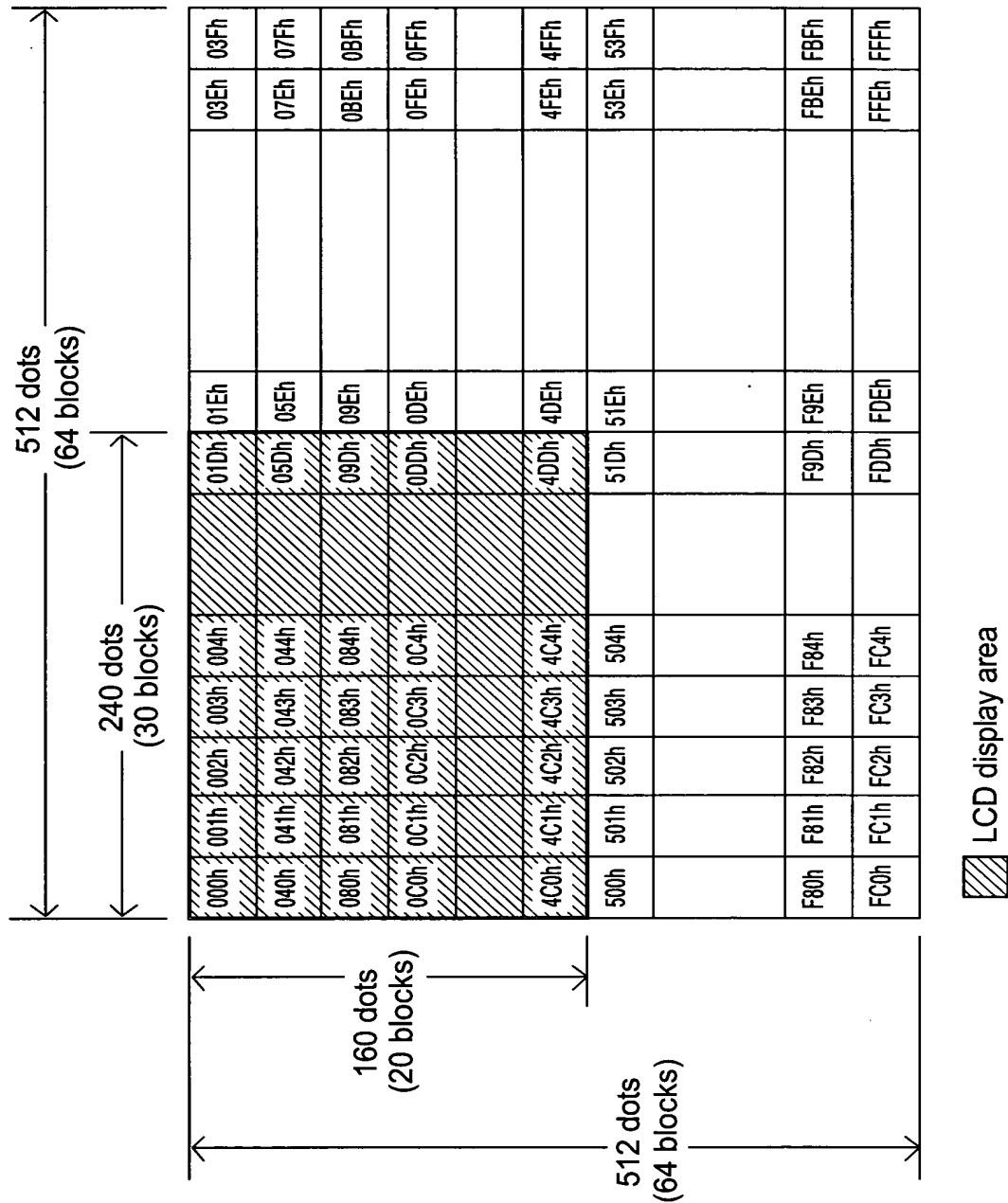
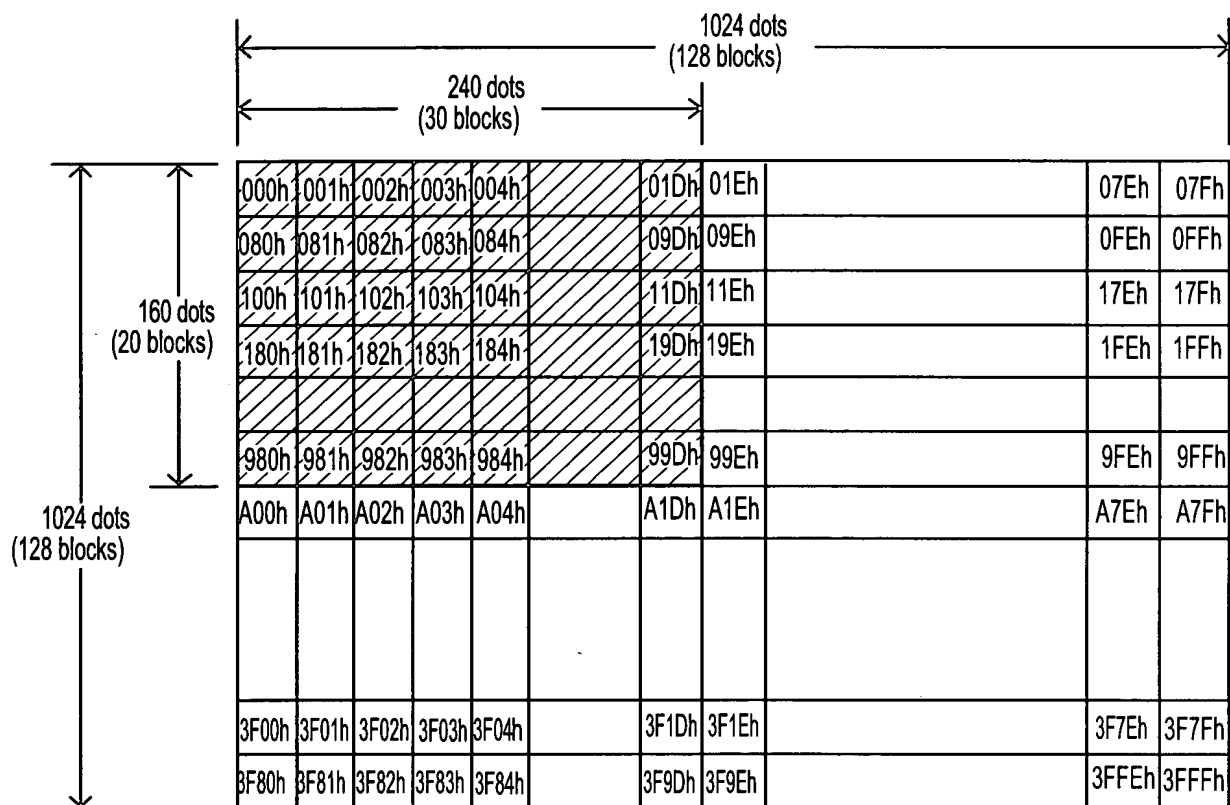


Fig.41C



 LCD Display Area

Fig. 41D

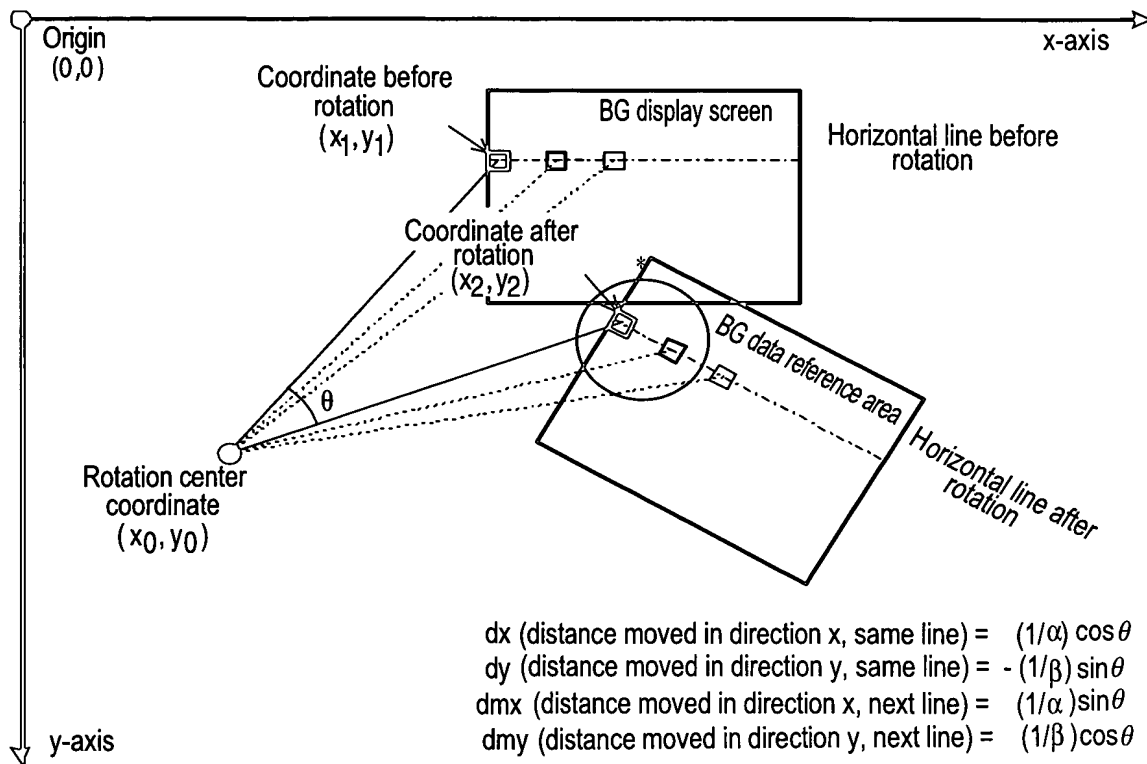


Fig. 42A

α : Magnification along x-axis
 β : Magnification along y-axis

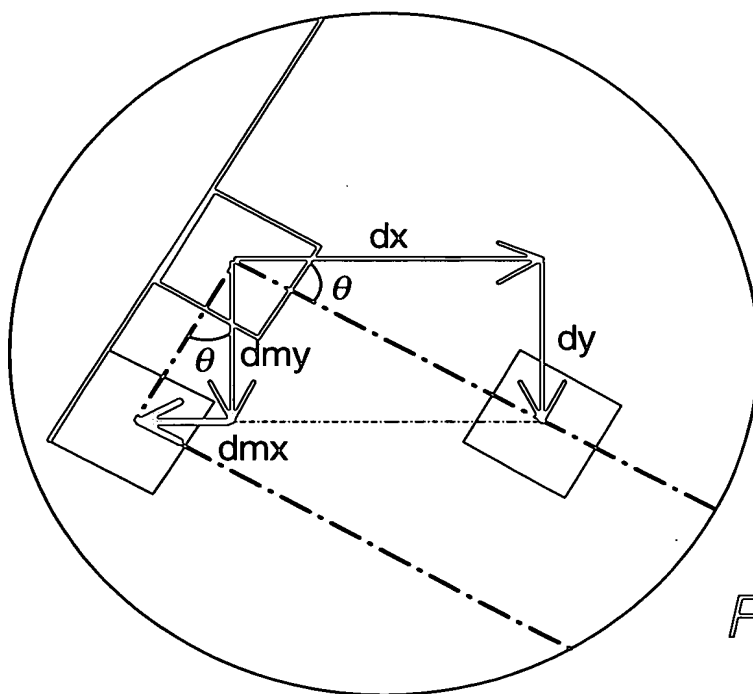


Fig. 42B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
028h	BG2X_L																	W	0000h
038h	BG3X_L																		

Fig.43A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
02Ah	BG2X_H																	W	0000h
03Ah	BG3X_H																		

Fig.43B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
02Ch	BG2Y_L																	W	0000h
03Ch	BG3Y_L																		

Fig.43C

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
02Eh	BG2Y_H																	W	0000h
03Eh	BG3Y_H																		

Fig.43D

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
020h	BG2PA																	W	0100h
030h	BG3PA																		

Fig.44A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
022h	BG2PB																	W	0000h
032h	BG3PB																		

Fig.44B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
024h	BG2PC																	W	0000h
034h	BG3PC																		

Fig.44C

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
026h	BG2PD																	W	0100h
036h	BG3PD																		

Fig.44D

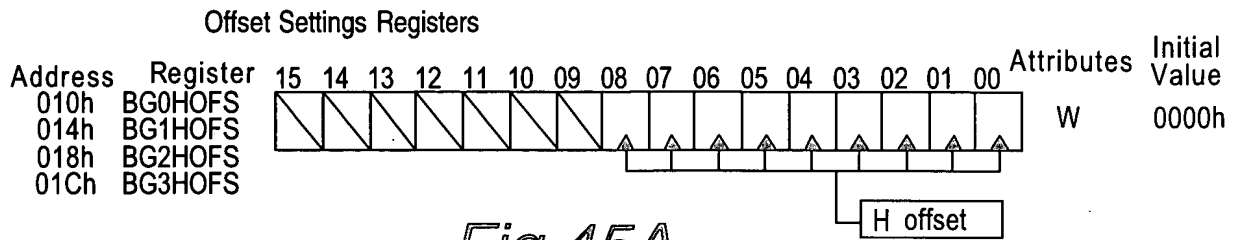


Fig.45A

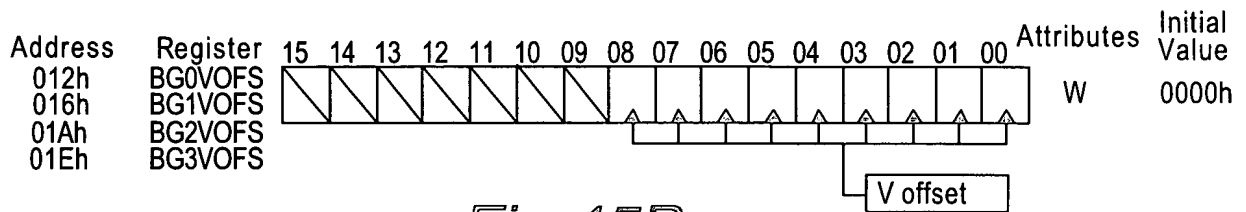


Fig.45B

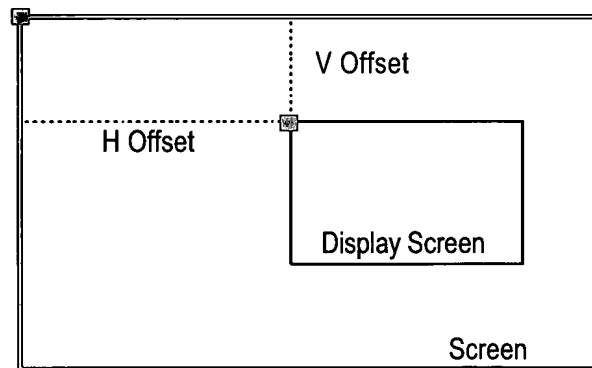


Fig.46

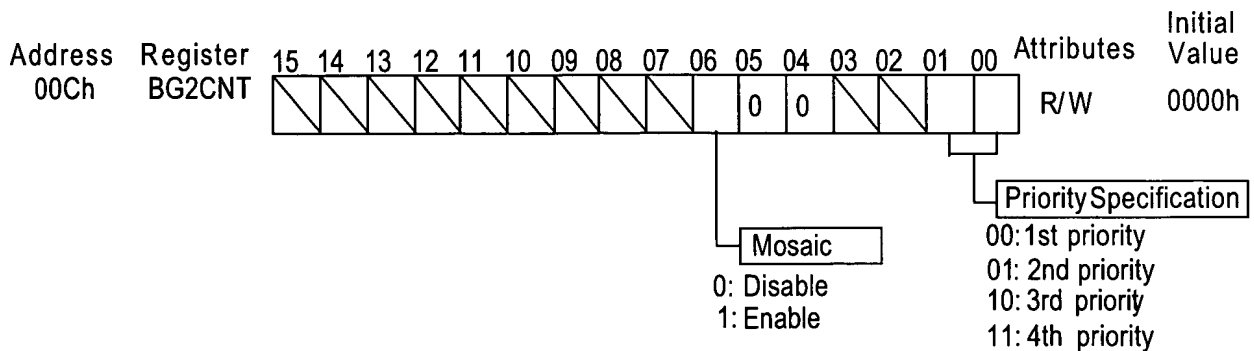


Fig.47

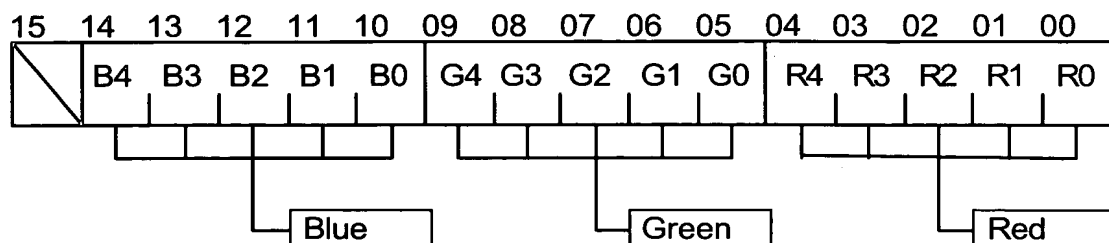


Fig. 48A

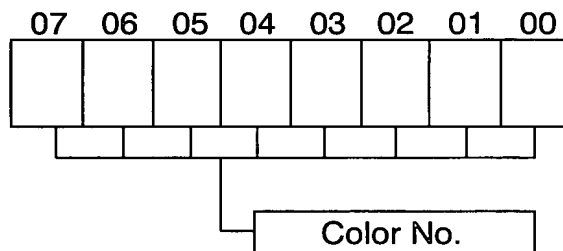


Fig. 48B

	0	1	2	3	4	...	236	237	238	239
0	0h	2h	4h	6h	8h	...	1D8h	1Dah	1DCh	1DEh
1	1E0h	1E2h	1E4h	1E6h	1E8h	...	3B8h	3Bah	3BCh	3BEh
2	3C0h	3C2h	3C4h	3C6h	3C8h	...	598h	59Ah	59Ch	59Eh
3	5A0h	5A2h	5A4h	5A6h	5A8h	...	778h	77Ah	77Ch	7Eh
4	780h	782h	784h	786h	788h	...	958h	95Ah	95Ch	95Eh
156	12480h	12482h	12484h	12486h	12488h	...	12658h	1265Ah	1265Ch	1265Eh
157	12660h	12662h	12664h	12666h	12668h	...	12838h	1283Ah	1283Ch	1283Eh
158	12840h	12842h	12844h	12846h	12848h	...	12A18h	12A1Ah	12A1Ch	12A1Eh
159	12A20h	12A22h	12A24h	12A26h	12A28h	...	12BF8h	12BFAh	12BFCh	12BFEh

VRAM address (+06000000h)

Fig. 49

SECRET 07162400

Frame 0

	0	1	2	3	4	...	236	237	238	239
0	0h	1h	2h	3h	4h	...	ECh	EDh	EEh	EFh
1	F0h	F1h	F2h	F3h	F4h	...	1DCh	1DDh	1DEh	1DFh
2	1E0h	1E1h	1E2h	1E3h	1E4h	...	2CCh	2CDh	2CEh	2CFh
3	2D0h	2D1h	2D2h	2D3h	2D4h	...	3BCh	3BDh	3BEh	3BFh
4	3C0h	3C1h	3C2h	3C3h	3C4h	...	4ACh	4ADh	4AEh	4AFh
156	9240h	9241h	9242h	9243h	9244h	...	932Ch	932Dh	932Eh	932Fh
157	9330h	9331h	9332h	9333h	9334h	...	941Ch	941Dh	941Eh	941Fh
158	9420h	9421h	9422h	9423h	9424h	...	950Ch	950Dh	950Eh	950Fh
159	9510h	9511h	9512h	9513h	9514h	...	95FCh	95FDh	95FEh	95FFh

VRAM address (+06000000h)

Fig. 50A

Frame 1

	0	1	2	3	4	...	236	237	238	239
0	A000h	A001h	A002h	A003h	A004h	...	A0ECh	A0EDh	A0EEh	A0EFh
1	A0F0h	A0F1h	A0F2h	A0F3h	A0F4h	...	A1DCh	A1DDh	A1DEh	A1DFh
2	A1E0h	A1E1h	A1E2h	A1E3h	A1E4h	...	A2CCh	A2CDh	A2CEh	A2CFh
3	A2D0h	A 2D1h	A2D2h	A 2D3h	A2D4h	...	A3BCh	A3BDh	A3BEh	A3BFh
4	A3C0h	A 3C1h	A3C2h	A 3C3h	A3C4h	...	A4ACh	A4ADh	A4AEh	A 4AFh
156	13240h	13241h	13242h	13243h	13244h	...	1332Ch	1332Dh	1332Eh	1332Fh
157	13330h	13331h	13332h	13333h	13334h	...	1341Ch	1341Dh	1341Eh	1341Fh
158	13420h	13421h	13422h	13423h	13424h	...	1350Ch	1350Dh	1350Eh	1350Fh
159	13510h	13511h	13512h	13513h	13514h	...	135FCh	135FDh	135FEh	135FFh

VRAM address (+06000000h)

Fig. 50B

Basic Character
8x8 dots
(16 colors/16 palettes)

000h	001h	002h	003h	004h	005h	006h	007h	008h	01Bh	01Ch	01Dh	01Eh	01Fh
020h	021h	022h	023h	024h	025h	026h	027h	028h	03Bh	03Ch	03Dh	03Eh	03Fh
040h	041h	042h	043h	044h	045h	046h	047h	048h	05Bh	05Ch	05Dh	05Eh	05Fh
060h	061h	062h	063h	064h	065h	066h	067h	068h	07Bh	07Ch	07Dh	07Eh	07Fh
080h	081h	082h	083h	084h	085h	086h	087h	088h	09Bh	09Ch	09Dh	09Eh	09Fh
0A0h	0A1h	0A2h	0A3h	0A4h	0A5h	0A6h	0A7h	0A8h	0BBh	0BCh	0BDh	0BEh	0BFh
0C0h	0C1h	0C2h	0C3h	0C4h	0C5h	0C6h	0C7h	0C8h	0DBh	0DCh	0DDh	0DEh	0DFh
0E0h	0E1h	0E2h	0E3h	0E4h	0E5h	0E6h	0E7h	0E8h	0FBh	0FCh	0FDh	0FEh	0FFh
100h	101h	102h	103h	104h	105h	106h	107h	108h	11Bh	11Ch	11Dh	11Eh	11Fh
120h	121h	122h	123h	124h	125h	126h	127h	128h	13Bh	13Ch	13Dh	13Eh	13Fh
140h	141h	142h	143h	144h	145h	146h	147h	148h	15Bh	15Ch	15Dh	15Eh	15Fh
160h	161h	162h	163h	164h	165h	166h	167h	168h	17Bh	17Ch	17Dh	17Eh	17Fh

Character mapping area (character no. in hexadecimal notation)

Character name

Fig. 52

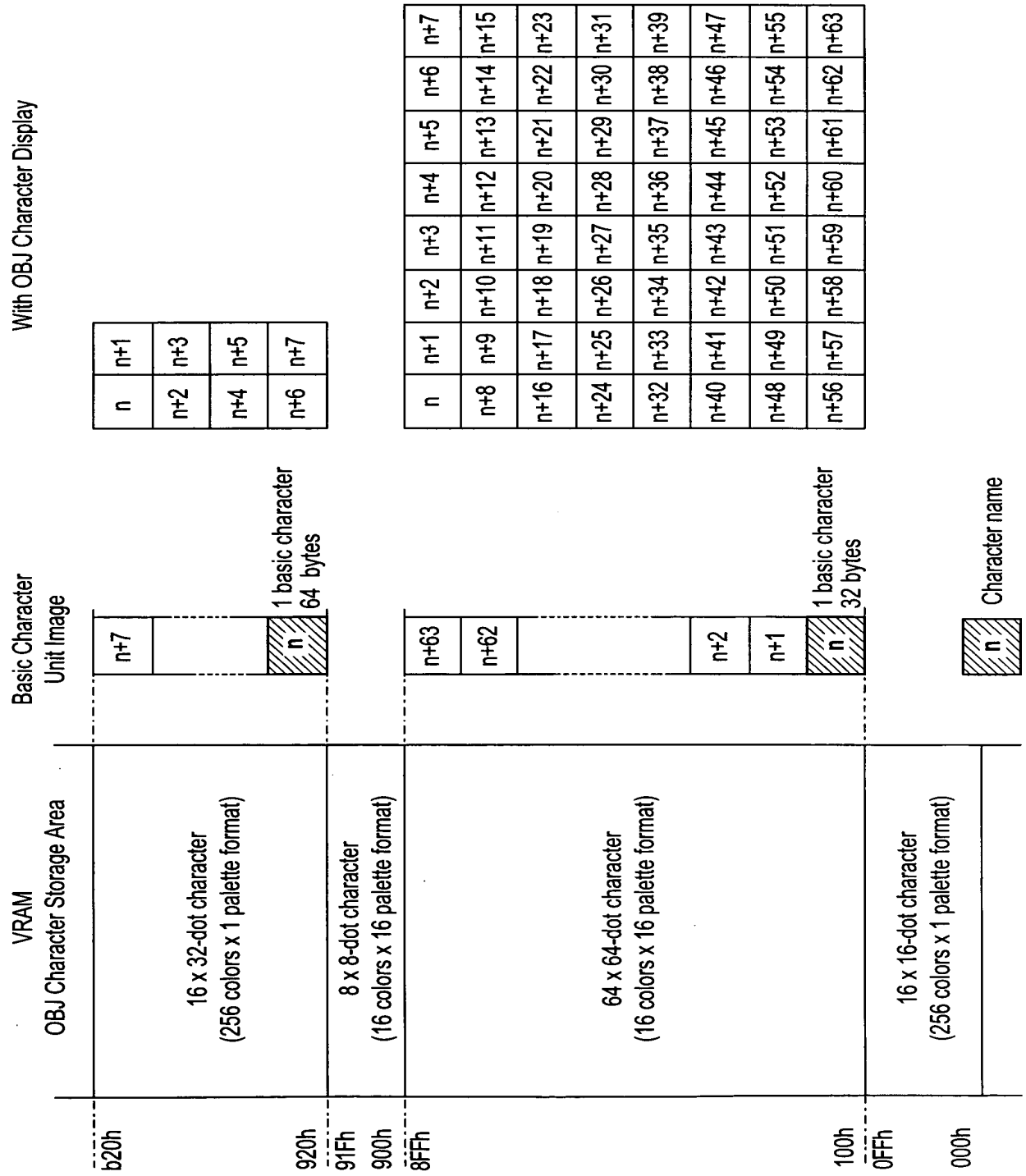


Fig. 53

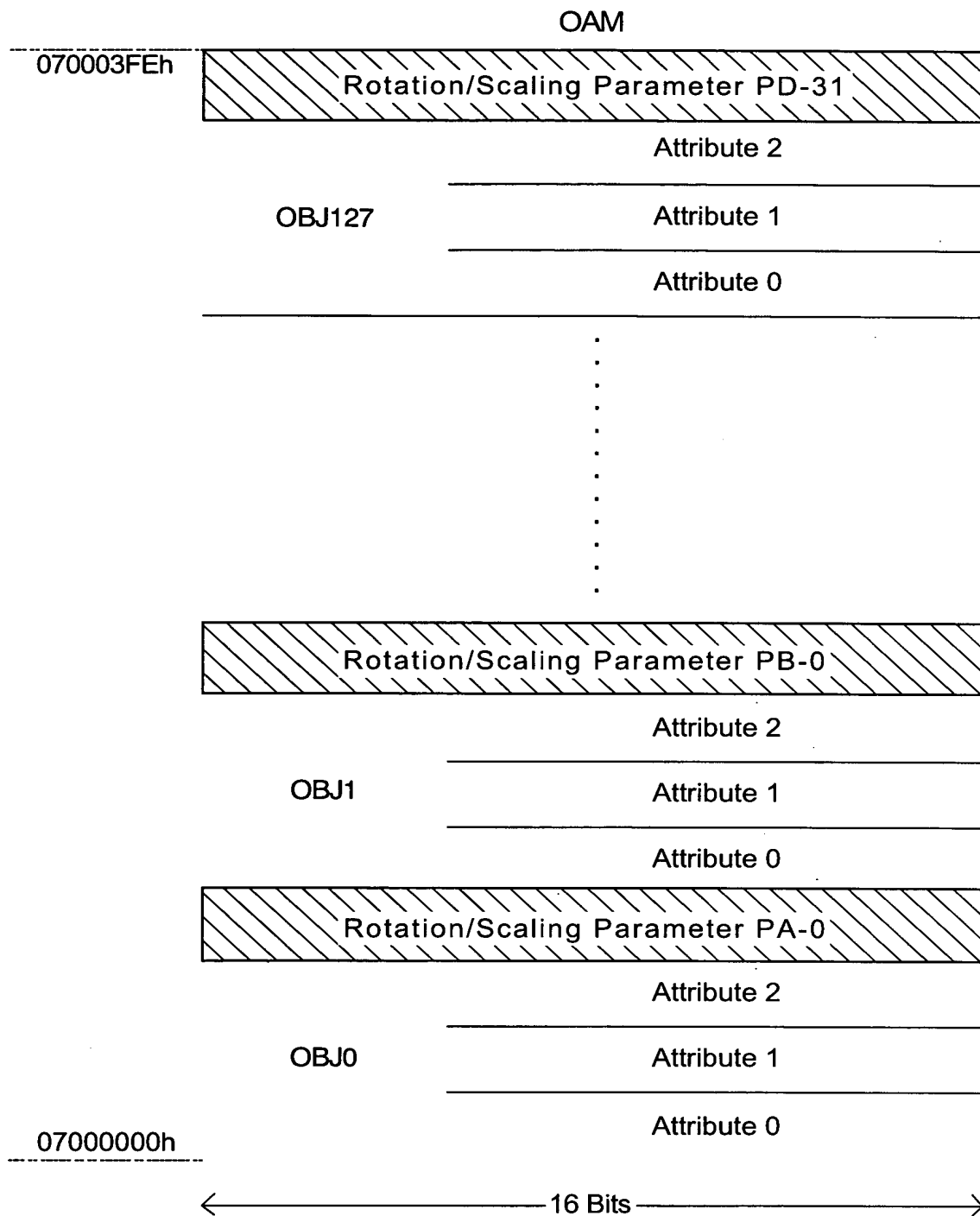
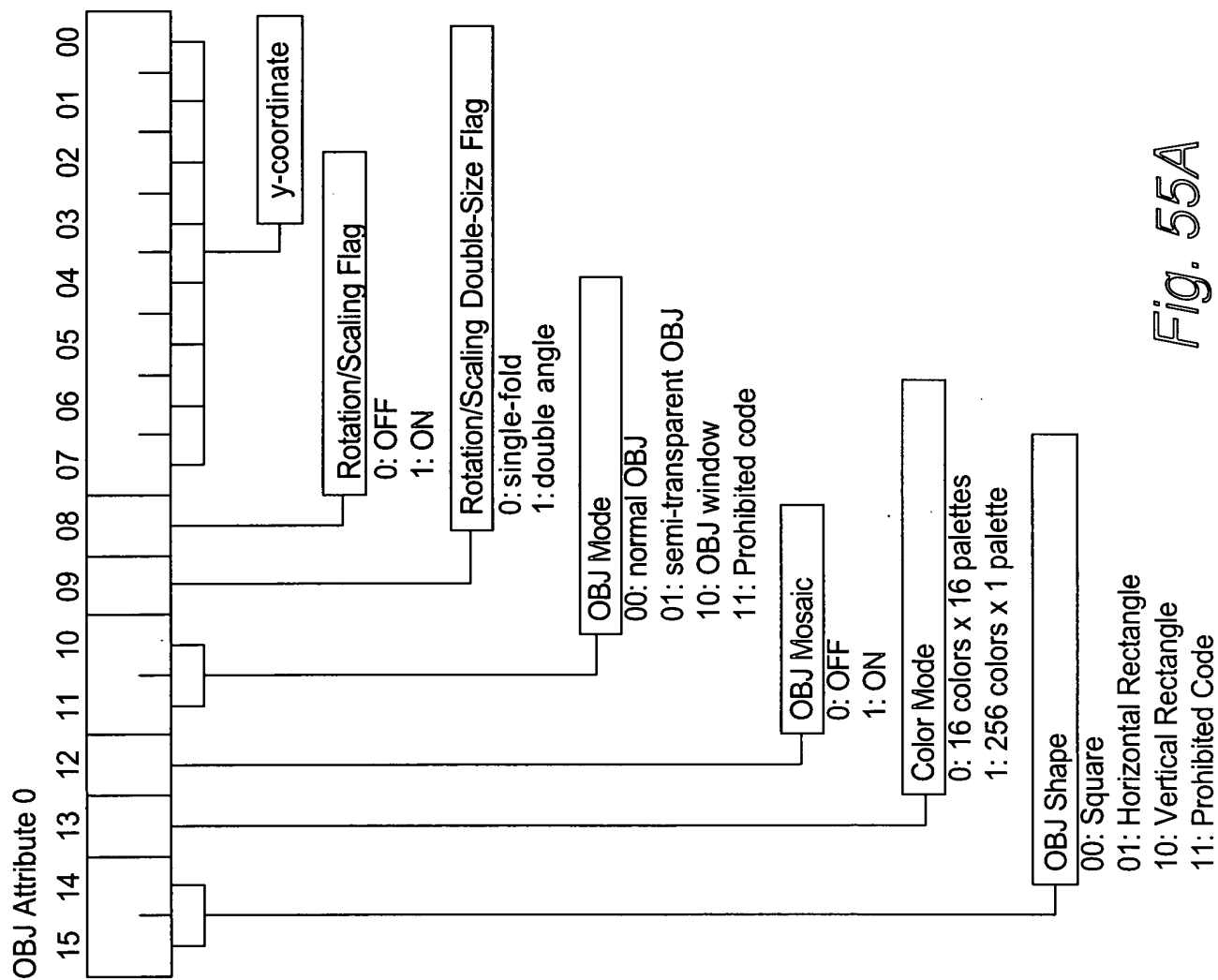


Fig. 54



OBJ Attribute 1

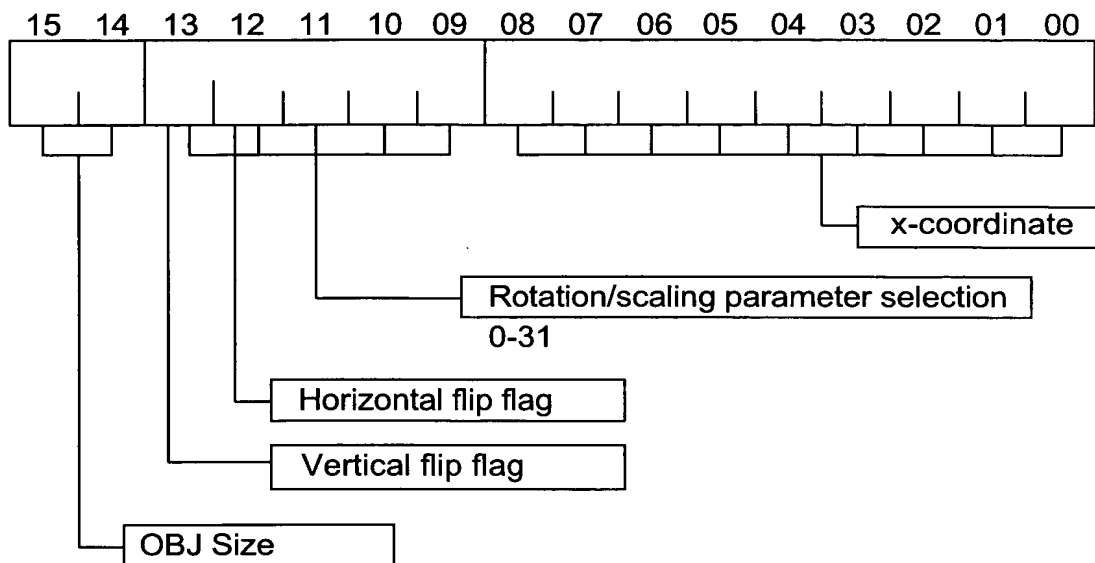


Fig. 55B

OBJ Attribute 2

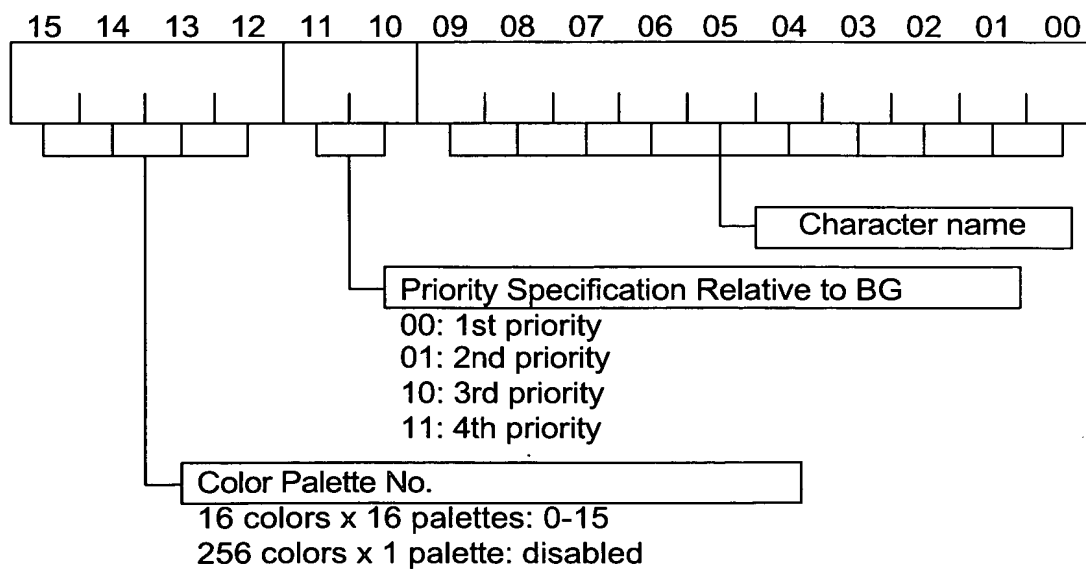


Fig. 55C

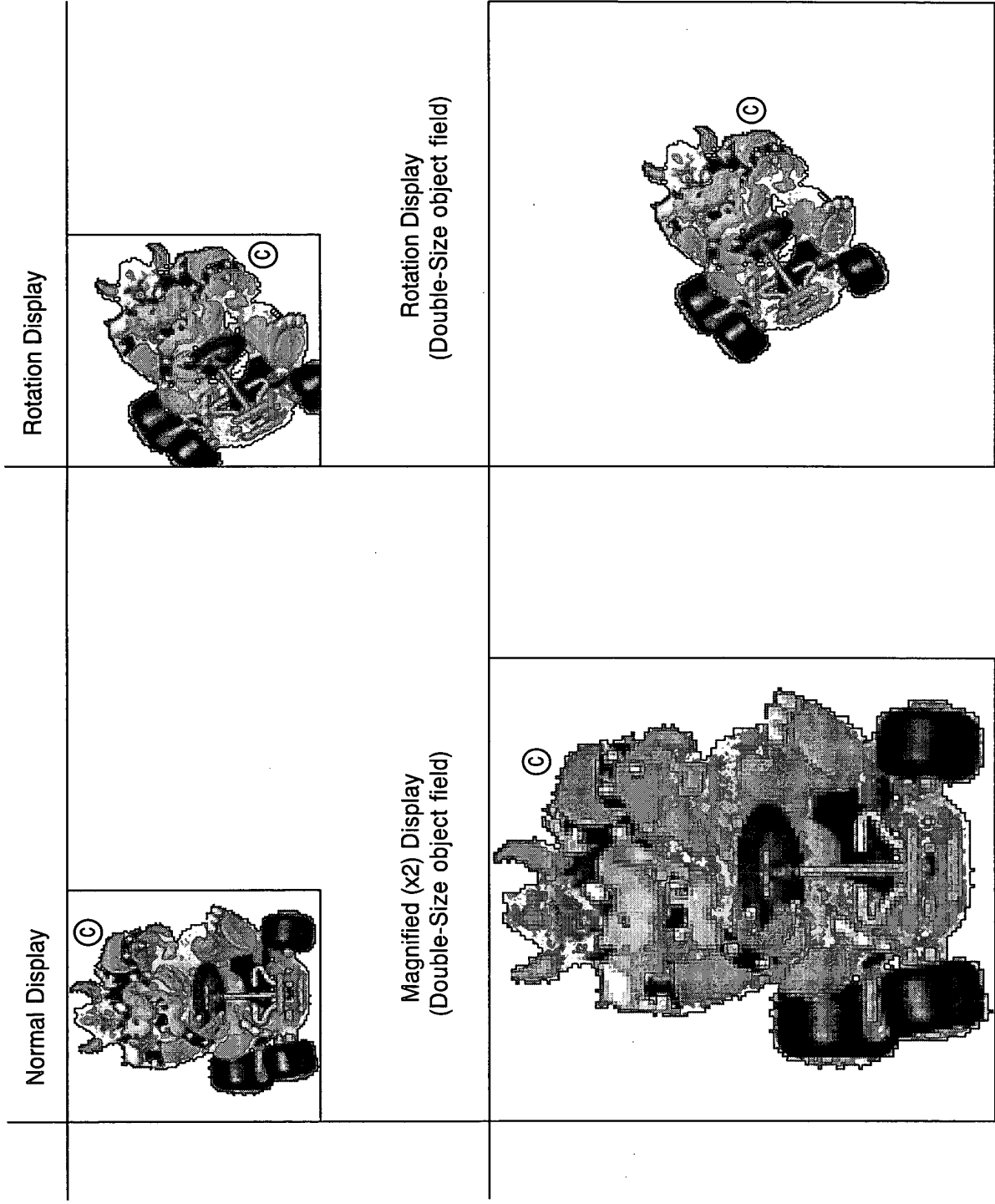


Fig. 56

[illegible]

OBJ Shape	OBJ Size			OBJ
	00	01	10	11
Square 00	A 8x8	B 16x16	C 32x32	D 64x64
Horizontal Rectangle 01	E 16x8	F 32x8	G 32x16	H 64x32
Vertical Rectangle 10	I 8x16	J 8x32	K 16x32	L 32x64
Prohibited Code 11				

Fig. 57

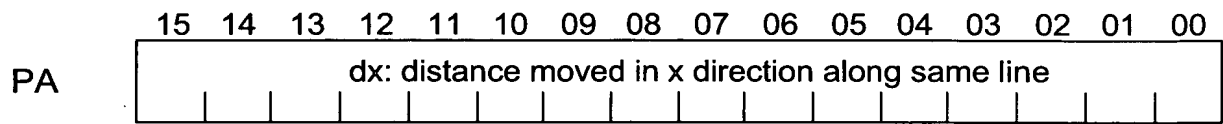


Fig. 59A

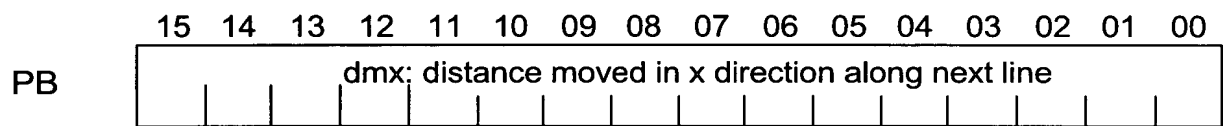


Fig. 59B

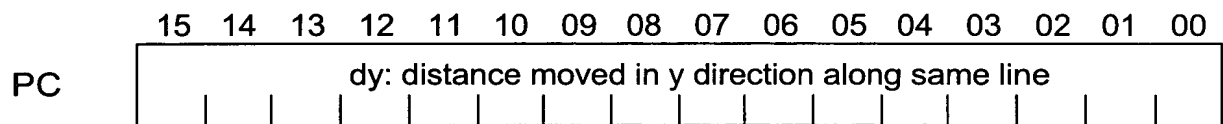


Fig. 59C

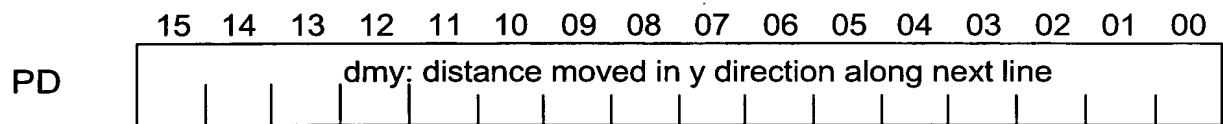


Fig. 59D

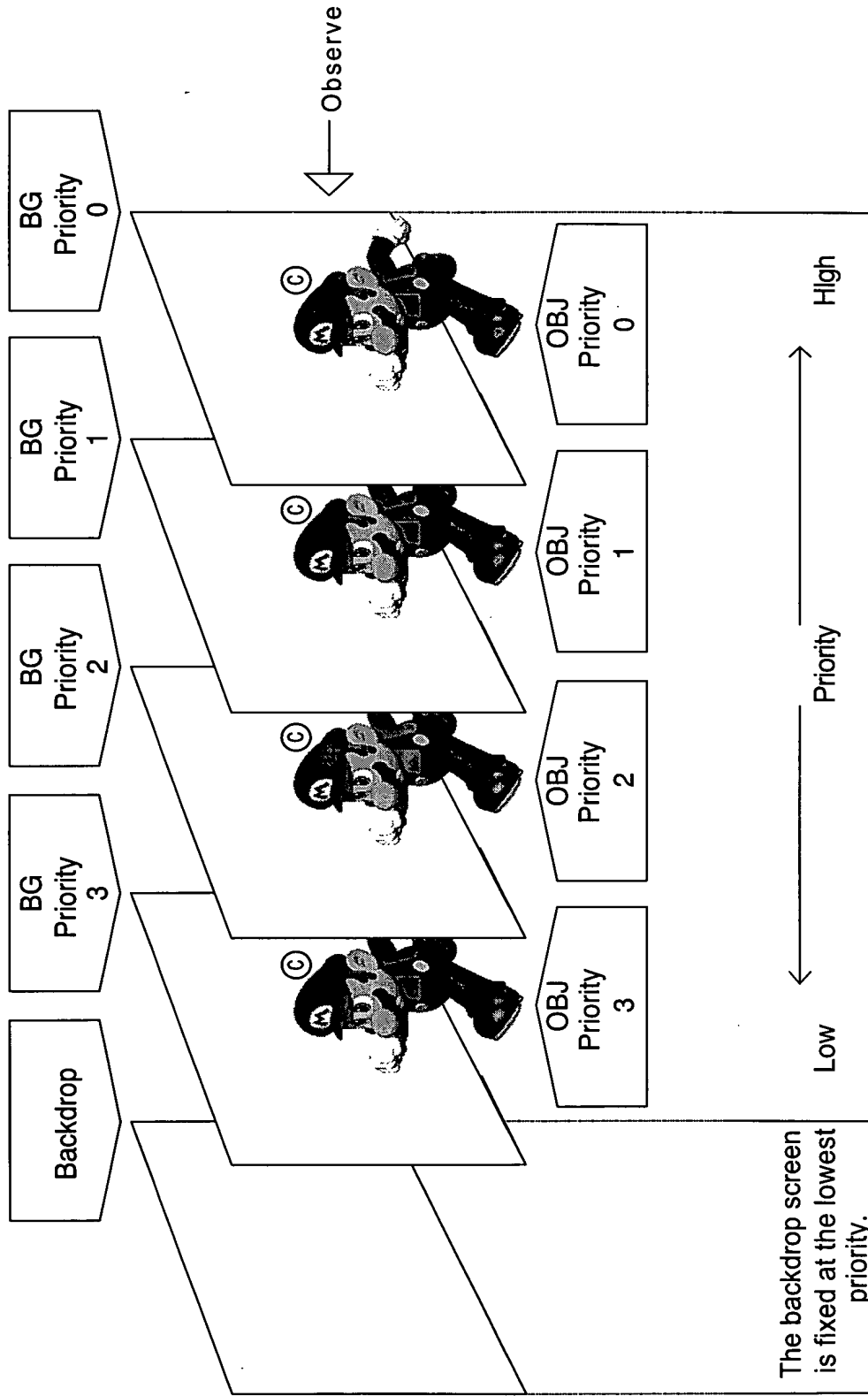


Fig. 60

00000000h
00000001h
00000002h
00000003h
00000004h
00000005h
00000006h
00000007h
00000008h
00000009h
0000000Ah
0000000Bh
0000000Ch
0000000Dh
0000000Eh
0000000Fh
00000010h
00000011h
00000012h
00000013h
00000014h
00000015h
00000016h
00000017h
00000018h
00000019h
0000001Ah
0000001Bh
0000001Ch
0000001Dh
0000001Eh
0000001Fh
00000020h
00000021h
00000022h
00000023h
00000024h
00000025h
00000026h
00000027h
00000028h
00000029h
0000002Ah
0000002Bh
0000002Ch
0000002Dh
0000002Eh
0000002Fh
00000030h
00000031h
00000032h
00000033h
00000034h
00000035h
00000036h
00000037h
00000038h
00000039h
0000003Ah
0000003Bh
0000003Ch
0000003Dh
0000003Eh
0000003Fh
00000040h
00000041h
00000042h
00000043h
00000044h
00000045h
00000046h
00000047h
00000048h
00000049h
0000004Ah
0000004Bh
0000004Ch
0000004Dh
0000004Eh
0000004Fh
00000050h
00000051h
00000052h
00000053h
00000054h
00000055h
00000056h
00000057h
00000058h
00000059h
0000005Ah
0000005Bh
0000005Ch
0000005Dh
0000005Eh
0000005Fh
00000060h
00000061h
00000062h
00000063h
00000064h
00000065h
00000066h
00000067h
00000068h
00000069h
0000006Ah
0000006Bh
0000006Ch
0000006Dh
0000006Eh
0000006Fh
00000070h
00000071h
00000072h
00000073h
00000074h
00000075h
00000076h
00000077h
00000078h
00000079h
0000007Ah
0000007Bh
0000007Ch
0000007Dh
0000007Eh
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00000080h
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00000088h
00000089h
0000008Ah
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0000008Fh
00000090h
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00000092h
00000093h
00000094h
00000095h
00000096h
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00000098h
00000099h
0000009Ah
0000009Bh
0000009Ch
0000009Dh
0000009Eh
0000009Fh
000000A0h
000000A1h
000000A2h
000000A3h
000000A4h
000000A5h
000000A6h
000000A7h
000000A8h
000000A9h
000000AAh
000000ABh
000000ACh
000000ADh
000000AEh
000000AFh
000000B0h
000000B1h
000000B2h
000000B3h
000000B4h
000000B5h
000000B6h
000000B7h
000000B8h
000000B9h
000000BAh
000000BBh
000000BCh
000000BDh
000000BEh
000000BFh
000000C0h
000000C1h
000000C2h
000000C3h
000000C4h
000000C5h
000000C6h
000000C7h
000000C8h
000000C9h
000000CAh
000000CBh
000000CCh
000000CDh
000000CEh
000000CFh
000000D0h
000000D1h
000000D2h
000000D3h
000000D4h
000000D5h
000000D6h
000000D7h
000000D8h
000000D9h
000000DAh
000000DBh
000000DCh
000000DDh
000000DEh
000000DFh
000000E0h
000000E1h
000000E2h
000000E3h
000000E4h
000000E5h
000000E6h
000000E7h
000000E8h
000000E9h
000000EAh
000000EBh
000000ECh
000000EDh
000000EEh
000000EFh
000000F0h
000000F1h
000000F2h
000000F3h
000000F4h
000000F5h
000000F6h
000000F7h
000000F8h
000000F9h
000000FAh
000000FBh
000000FCh
000000FDh
000000FEh
000000FFh

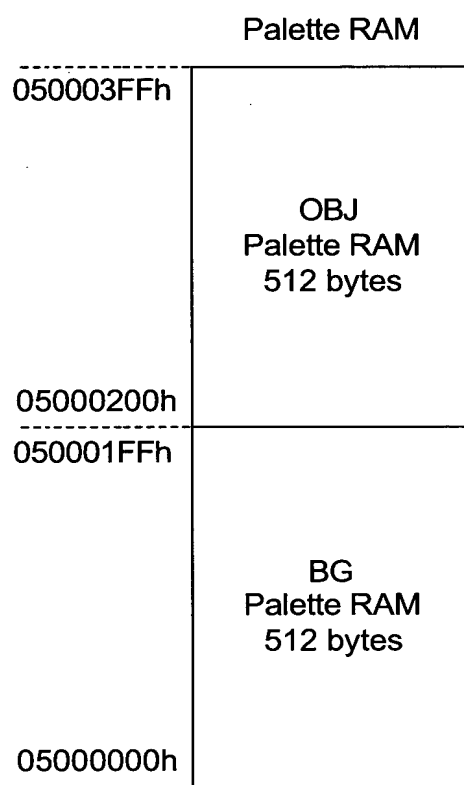


Fig. 61

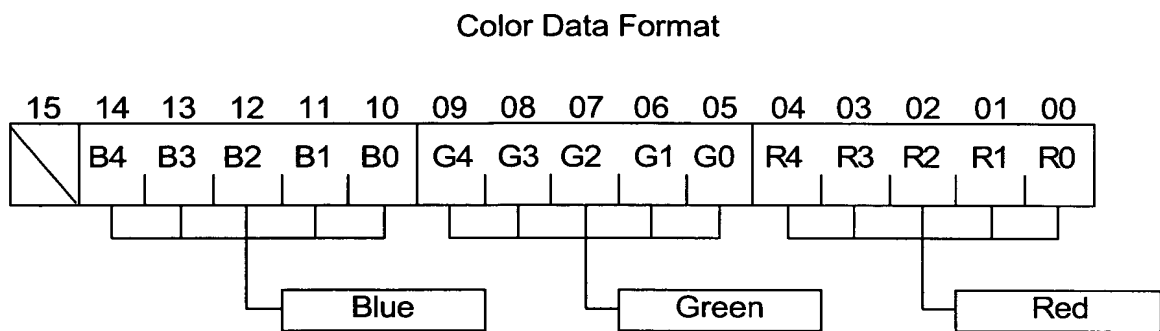


Fig. 63

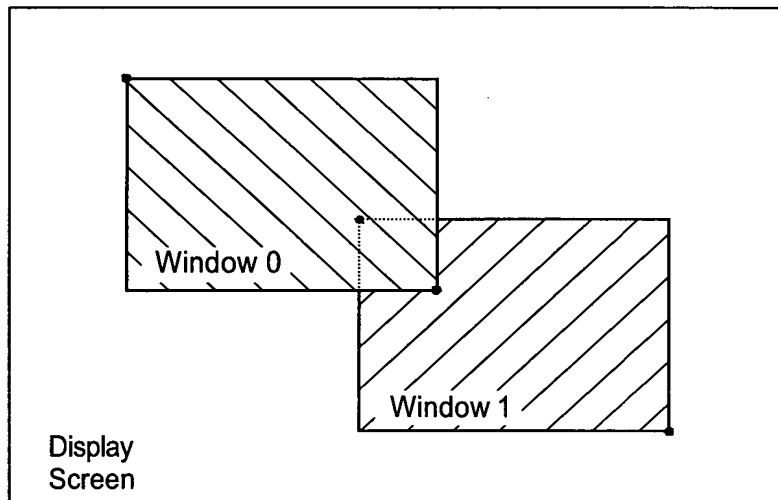


Fig. 64

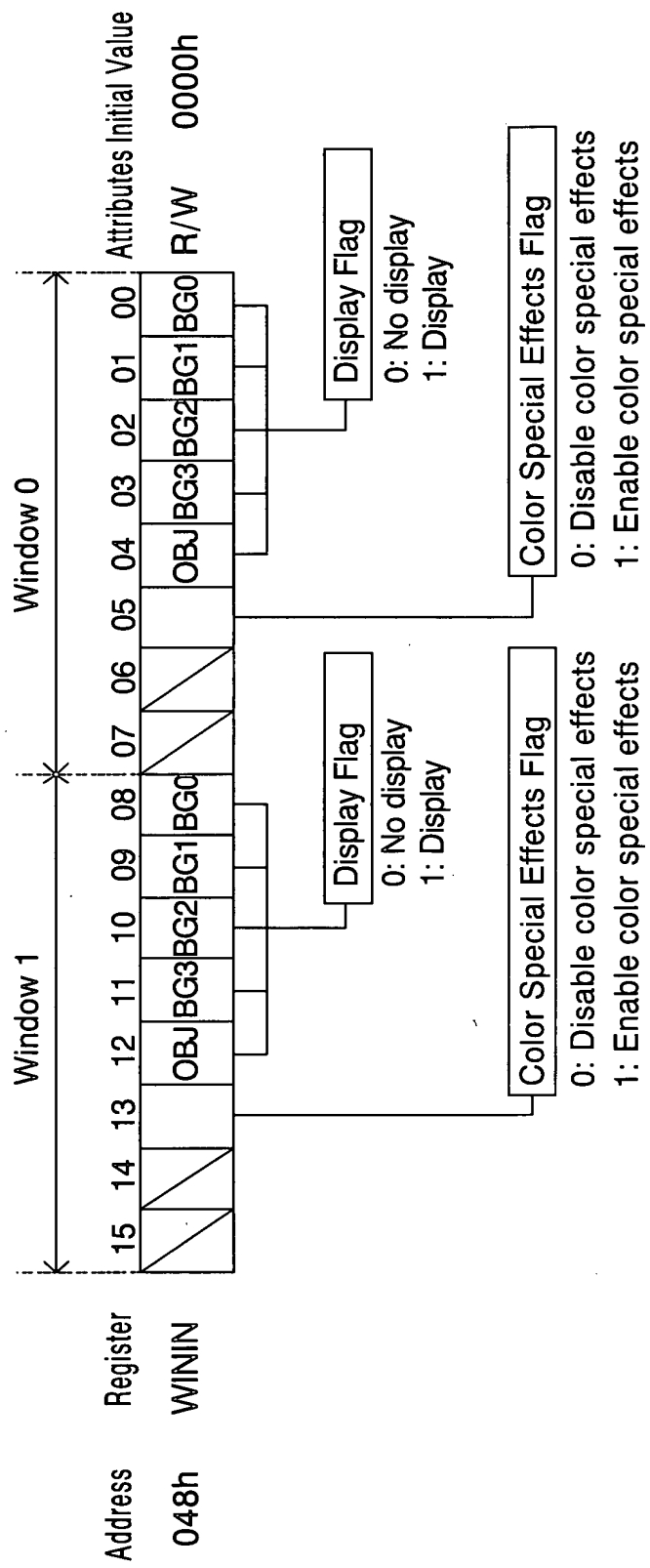


Fig. 65

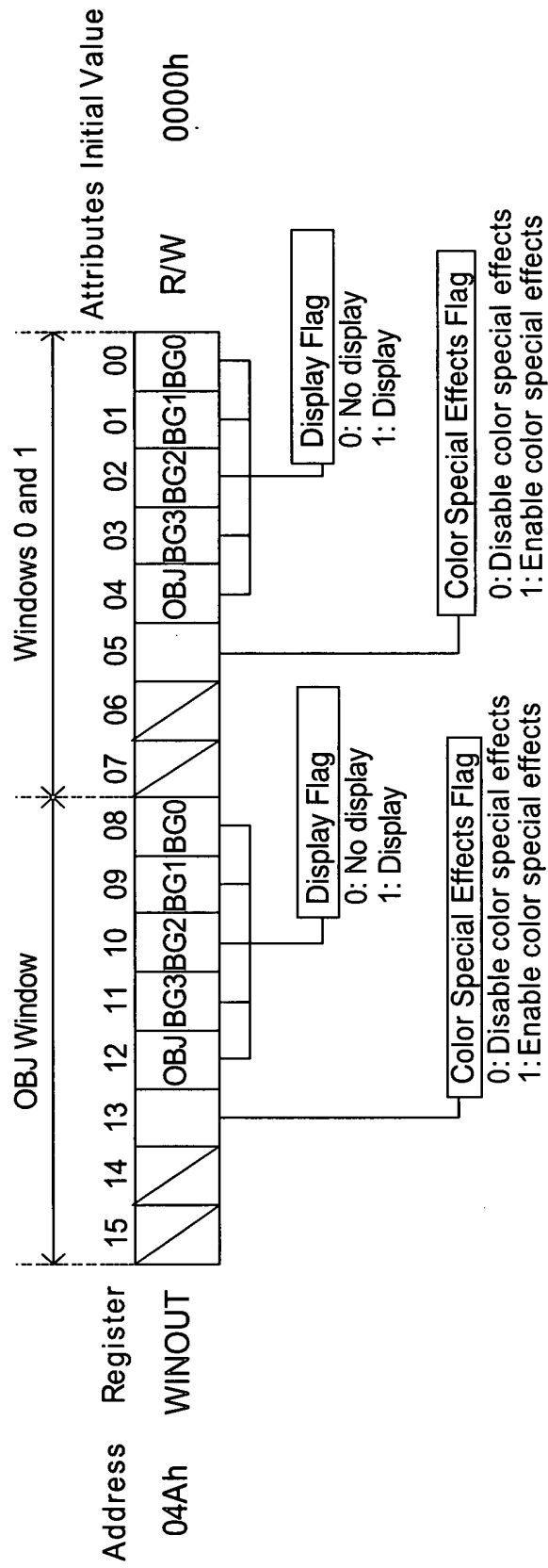


Fig. 66

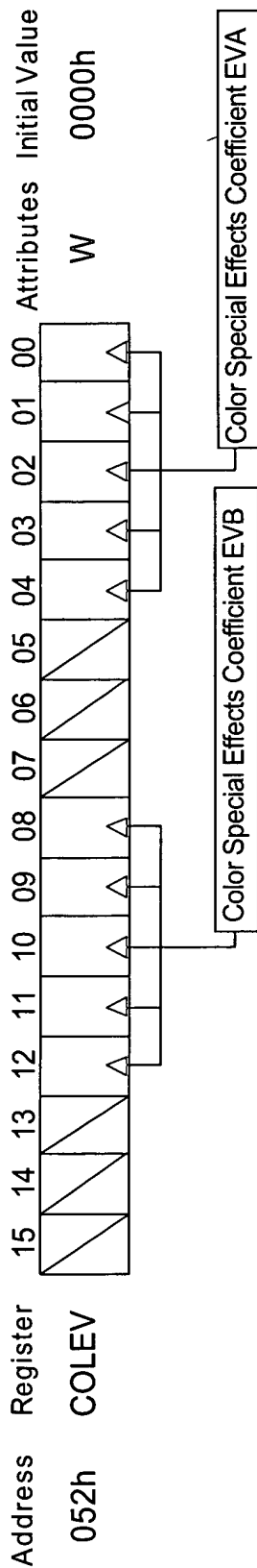


Fig. 68A

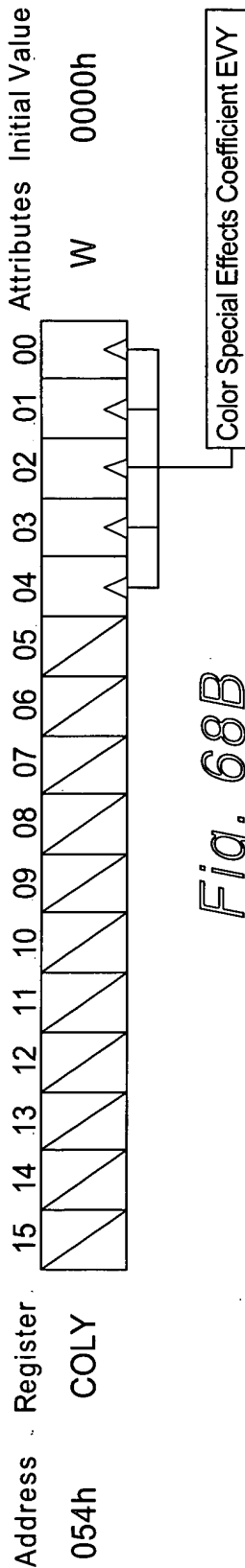


Fig. 68B

EVA, EVB, EVY			EVA, EVB, EVY			Coeff.			EVA, EVB, EVY			Coeff.		
0	0	0	0	0	0	0	0	0	1	0	0	0	8/16	8/16
0	0	0	0	1	1/16	1/16	0	0	1	0	0	1	9/16	9/16
0	0	0	1	0	2/16	2/16	0	1	0	0	1	0	10/16	10/16
0	0	0	1	1	3/16	3/16	0	1	0	1	1	1	11/16	11/16
0	0	1	0	0	4/16	4/16	0	1	1	0	0	0	12/16	12/16
0	0	1	0	1	5/16	5/16	0	1	1	0	1	0	13/16	13/16
0	0	1	1	0	6/16	6/16	0	1	1	1	0	0	14/16	14/16
0	0	1	1	1	7/16	7/16	0	1	1	1	1	1	15/16	15/16
1	1	1	1	1	1	1	1	1	1	1	1	1	16/16	16/16

Fig. 69

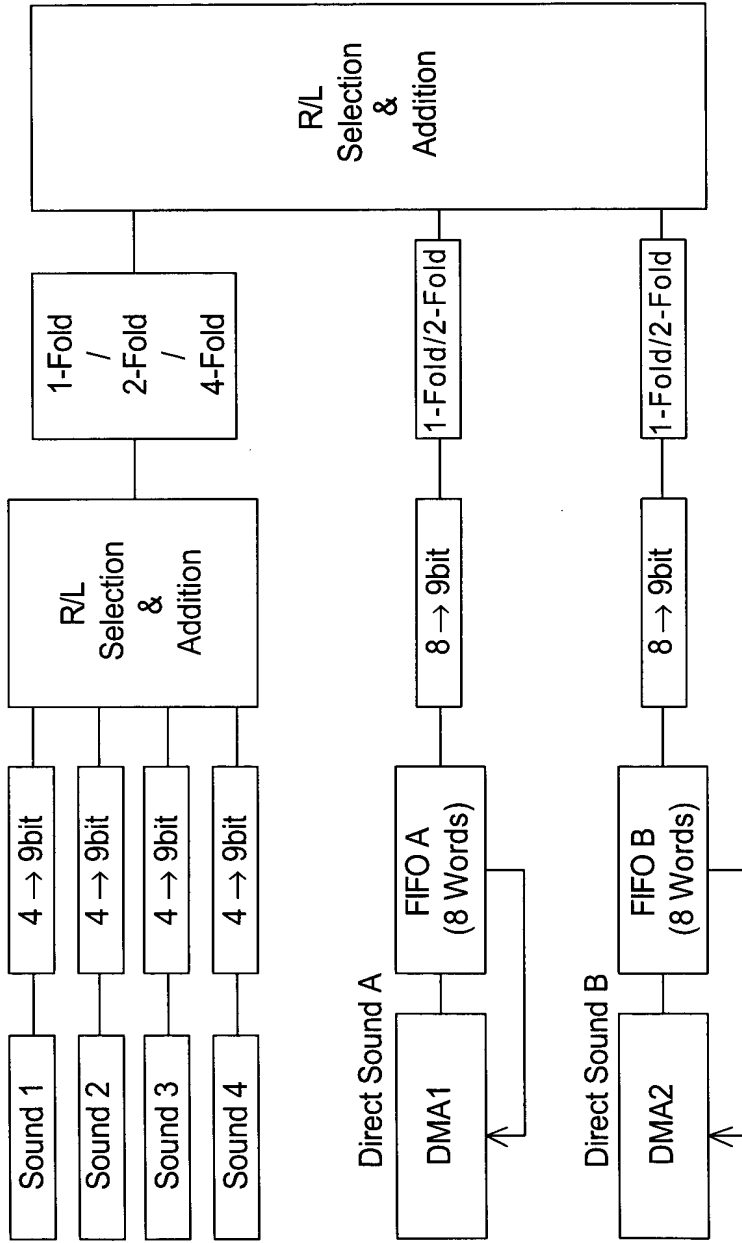


Fig. 70

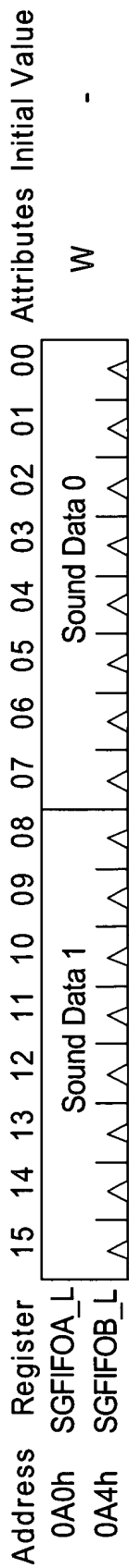


Fig. 71A

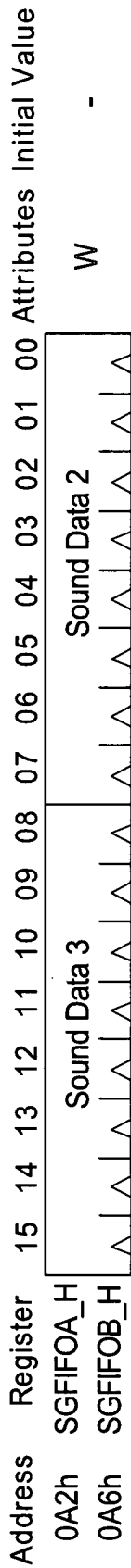


Fig. 71B

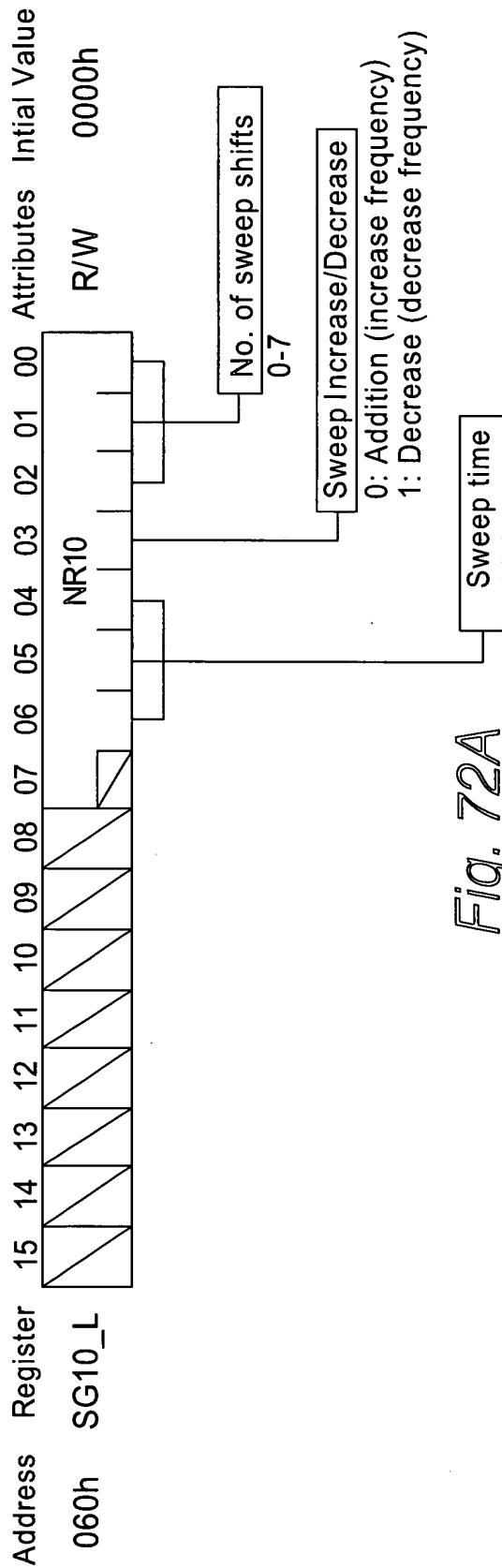


Fig. 72A

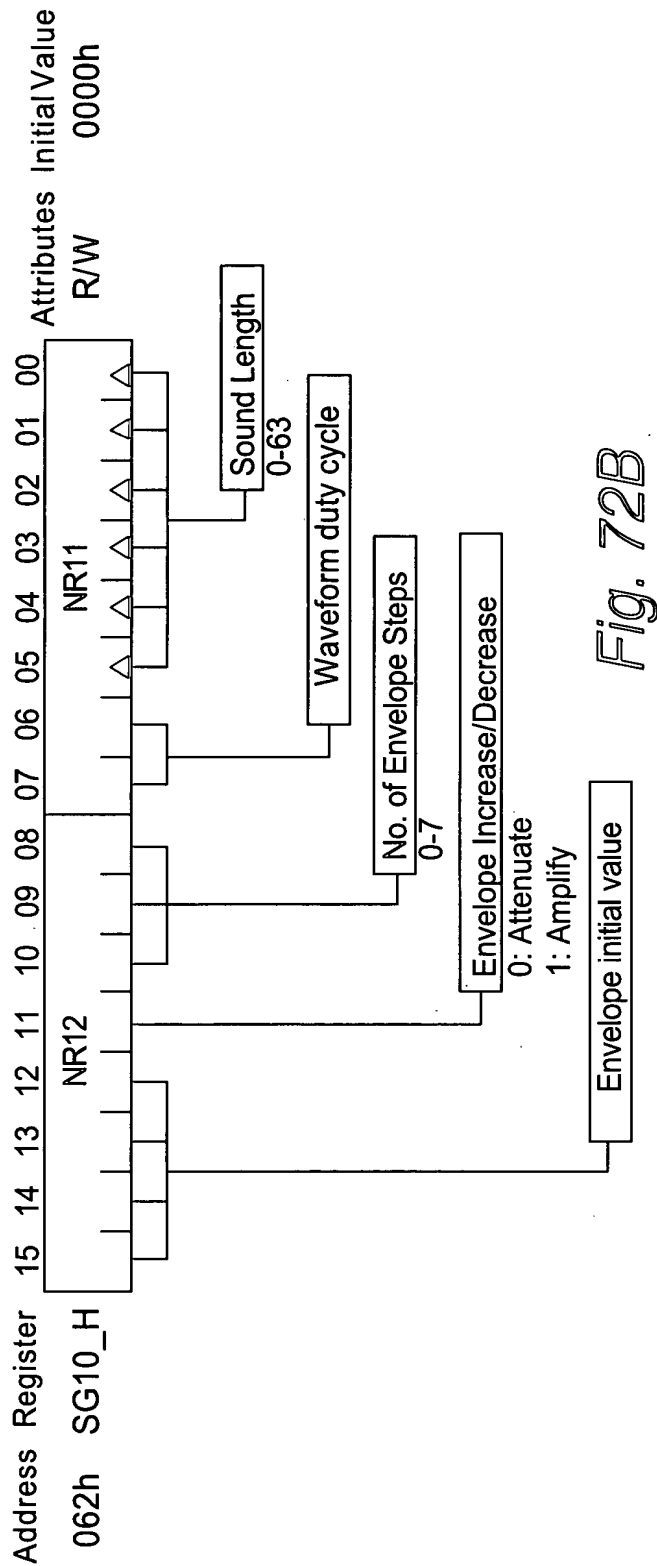


Fig. 72B

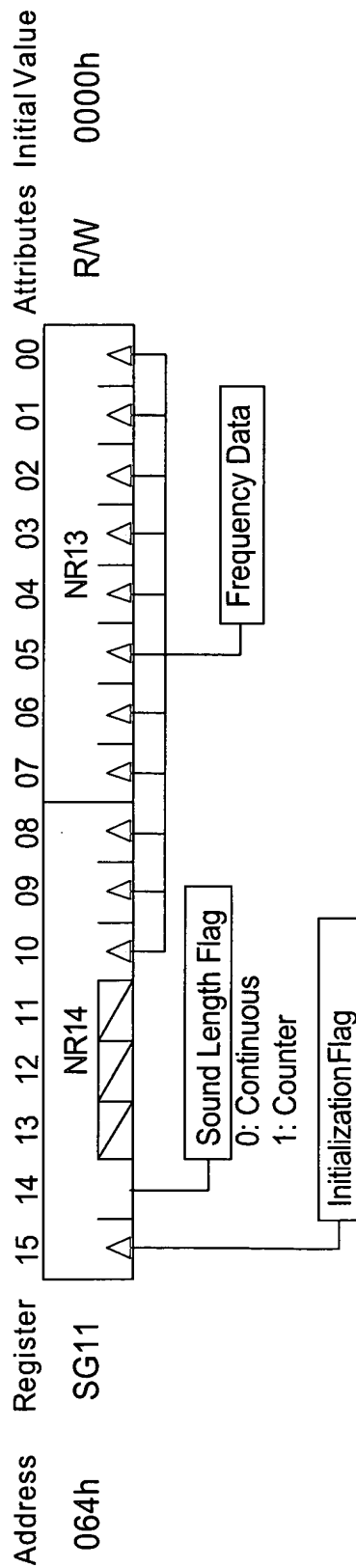


Fig. 72C

Setting	Duty Cycle	Waveform
00	12.5%	
01	25.0%	
10	50.0%	
11	75.0%	

Fig. 73

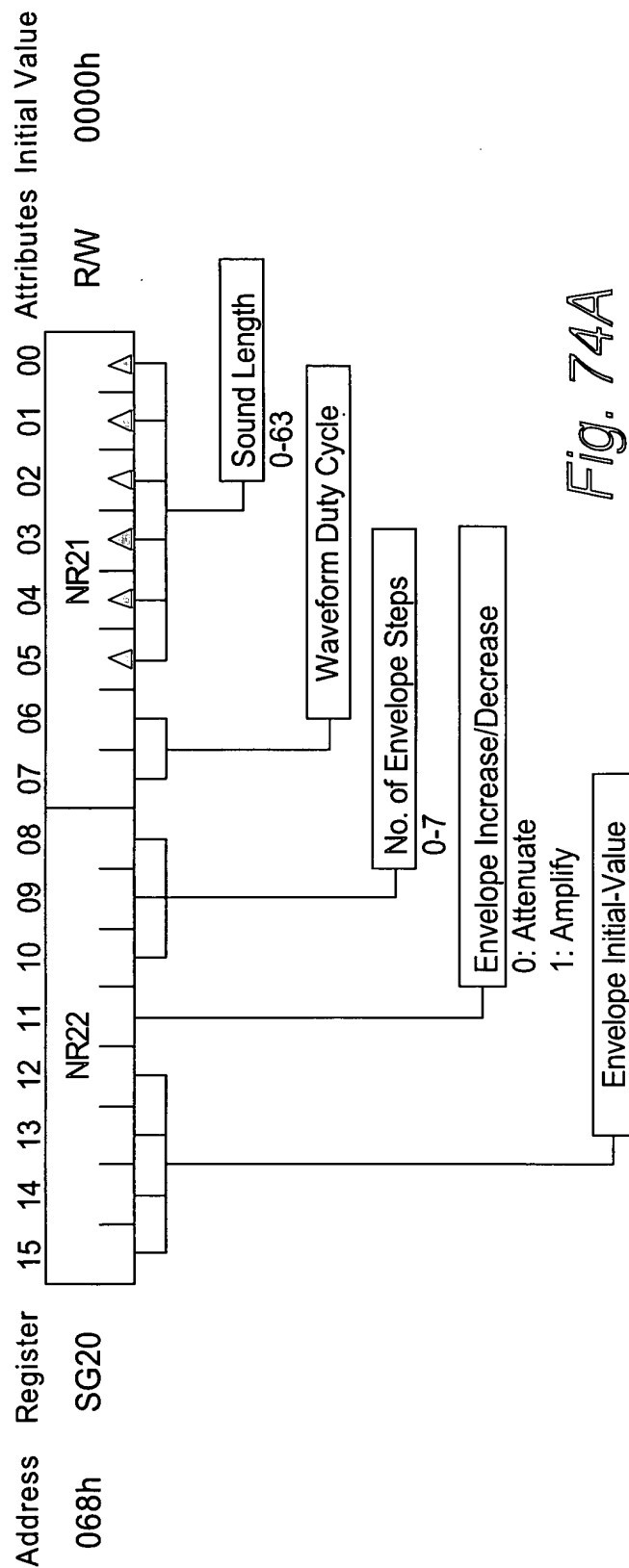


Fig. 74A

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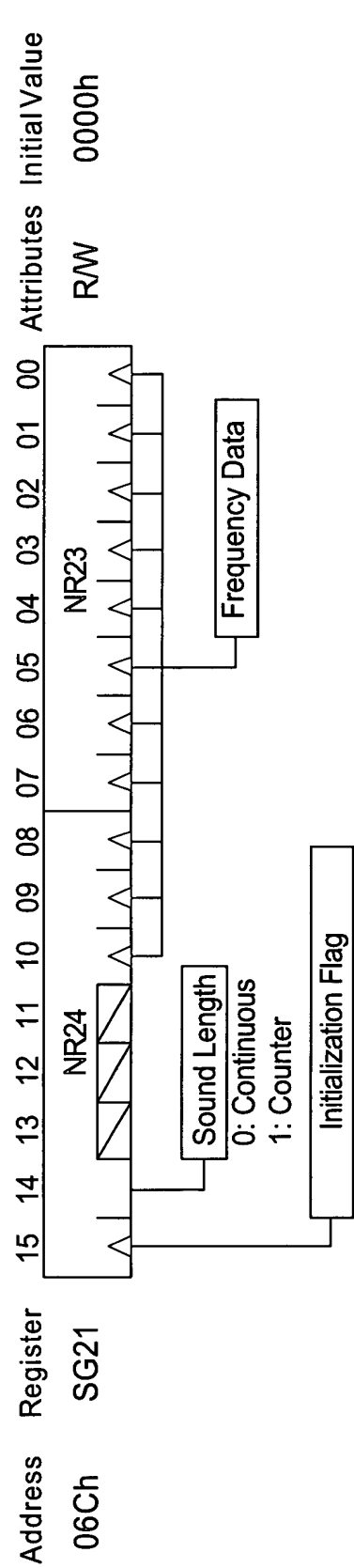


Fig. 74B

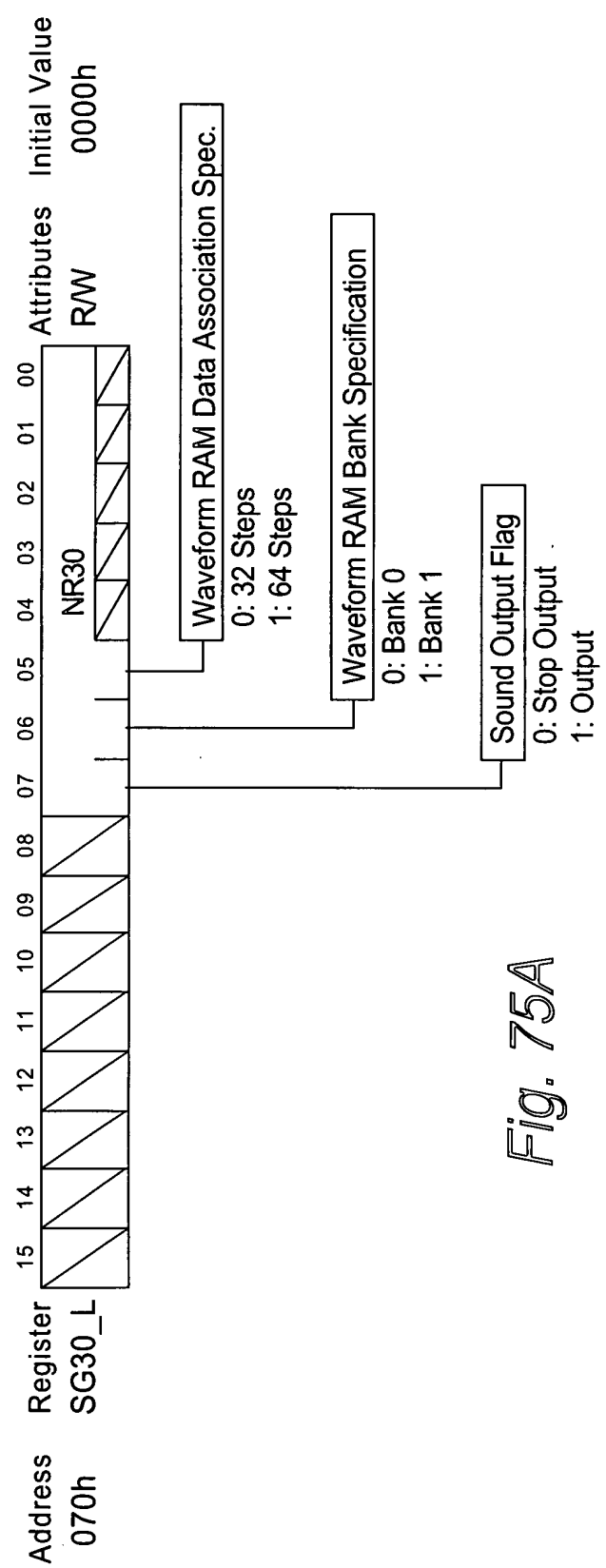


Fig. 75A

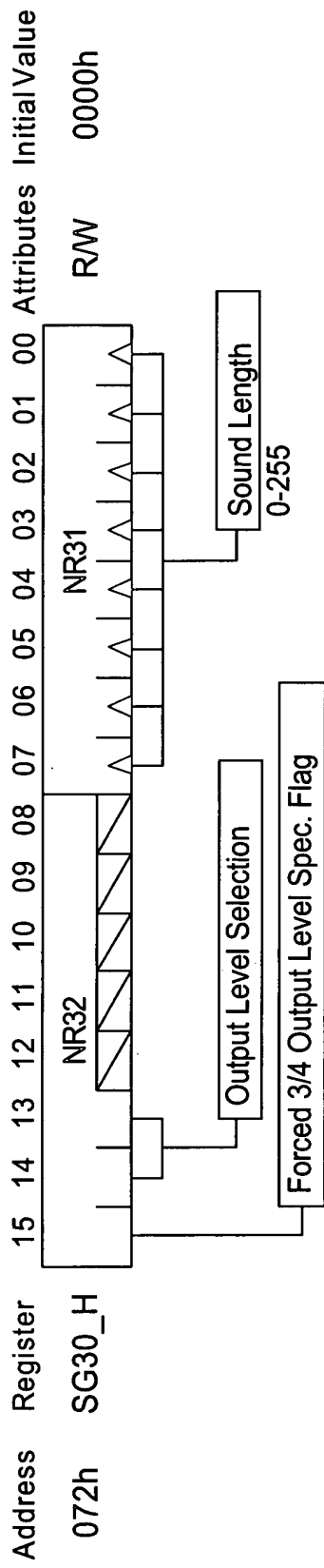


Fig. 75B

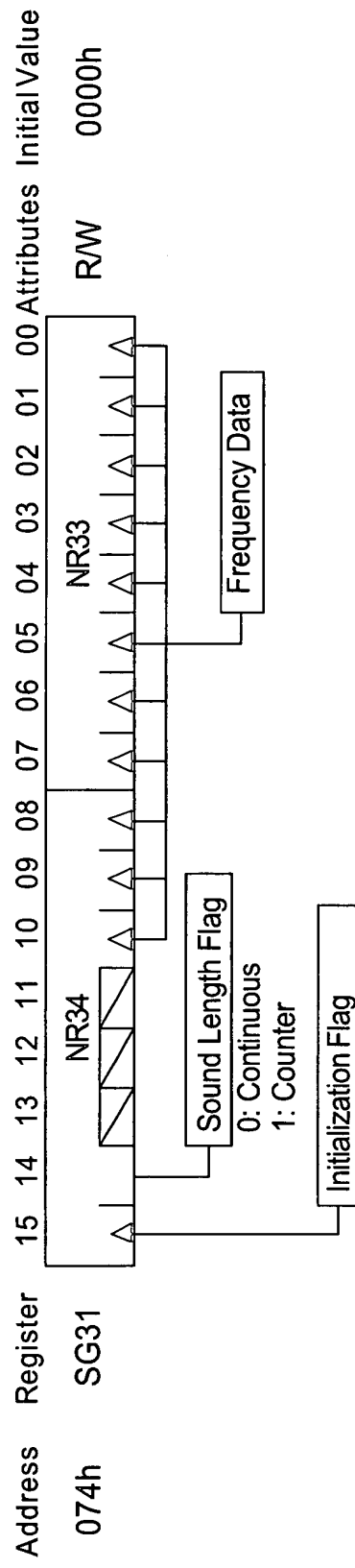


Fig. 75C

Address	Register																	Attributes	Initial Value				
098h	SGWR2_L	15	14	13	12	11	10	09	08	Step 19				Step 16				Step 17				R/W	-

Fig. 76E

Address	Register	Attributes																Initial Value
09Ah	SGWR2_H	R/W																-
		15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
		Step 22				Step 23				Step 20				Step 21				

Fig. 76F

Address	Register	Attributes																Initial Value					
09Ch	SGWR3_L	15	14	13	12	11	10	09	08	Step 27				Step 24				Step 25				R/W	-

Fig. 76G

Address	Register																	Attributes	Initial Value
09Eh	SGWR3_H	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	R/W	-
		Step 30				Step 31				Step 28				Step 29					

Fig. 76H

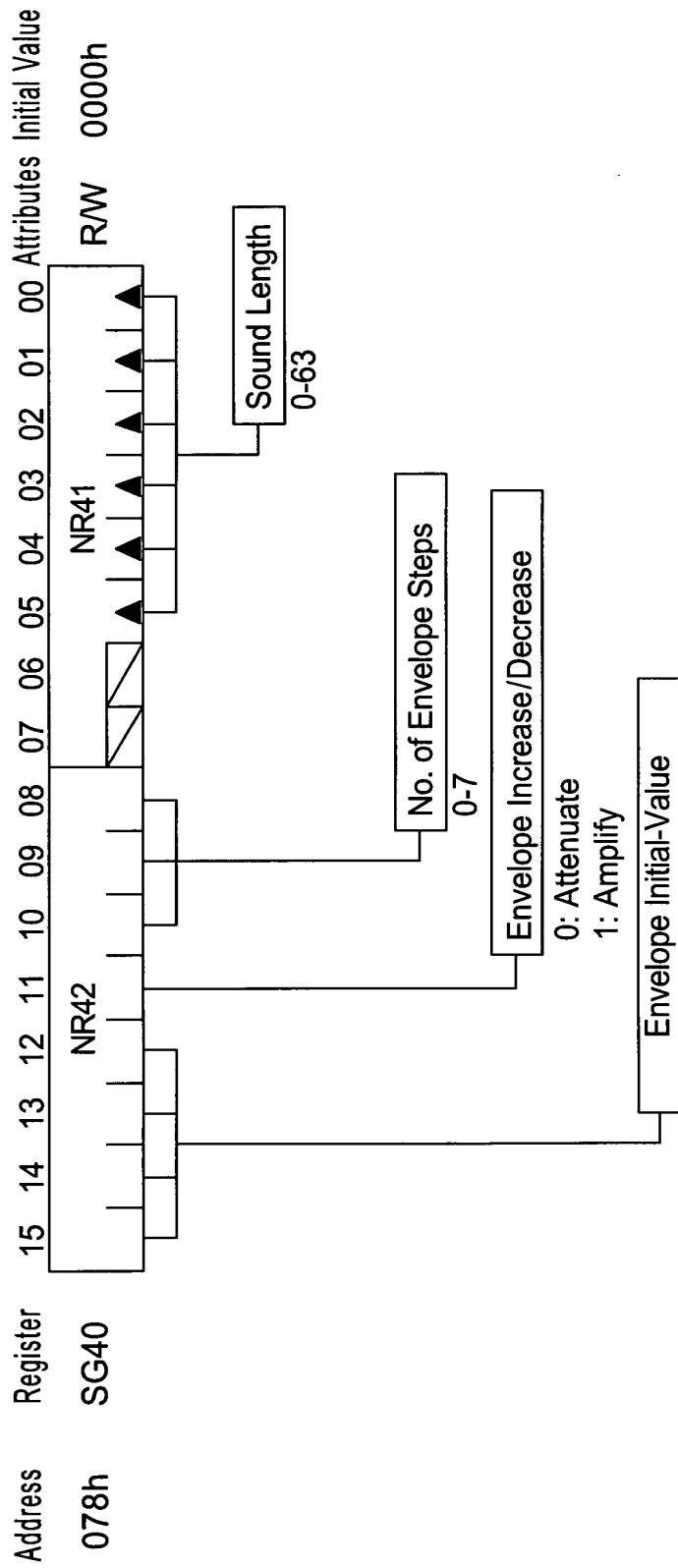


Fig. 77A

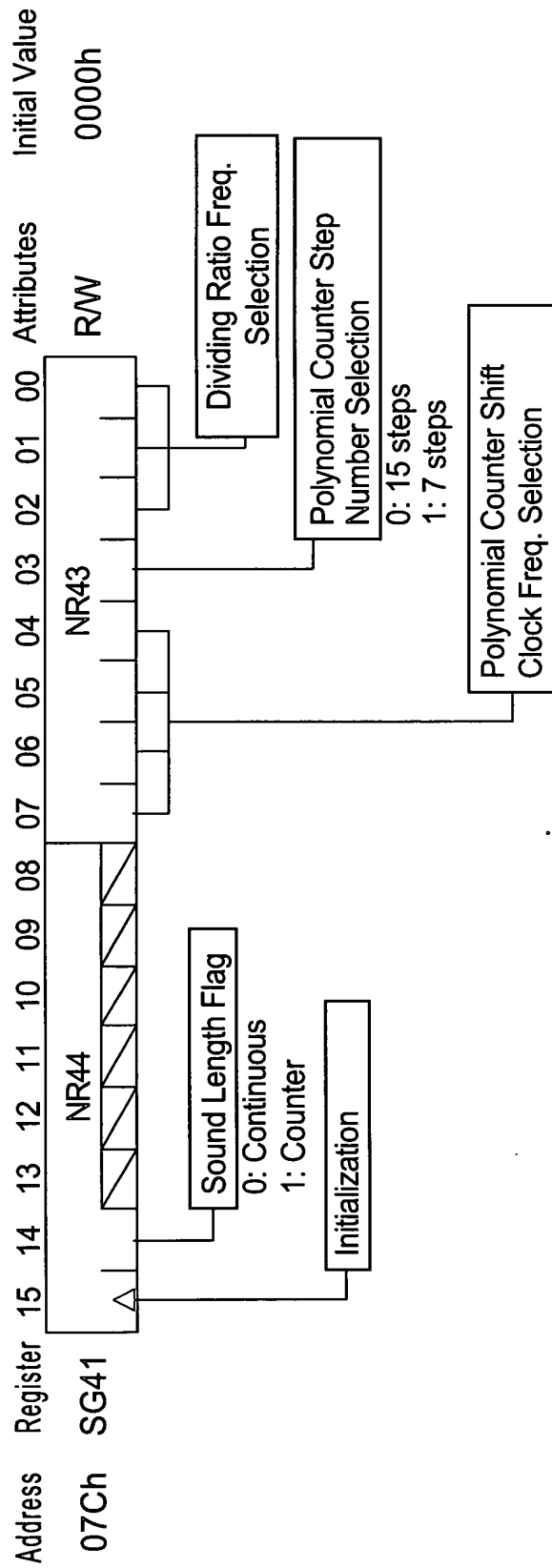


Fig. 77B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
082h	SGCNT0_H																	RW	0000h

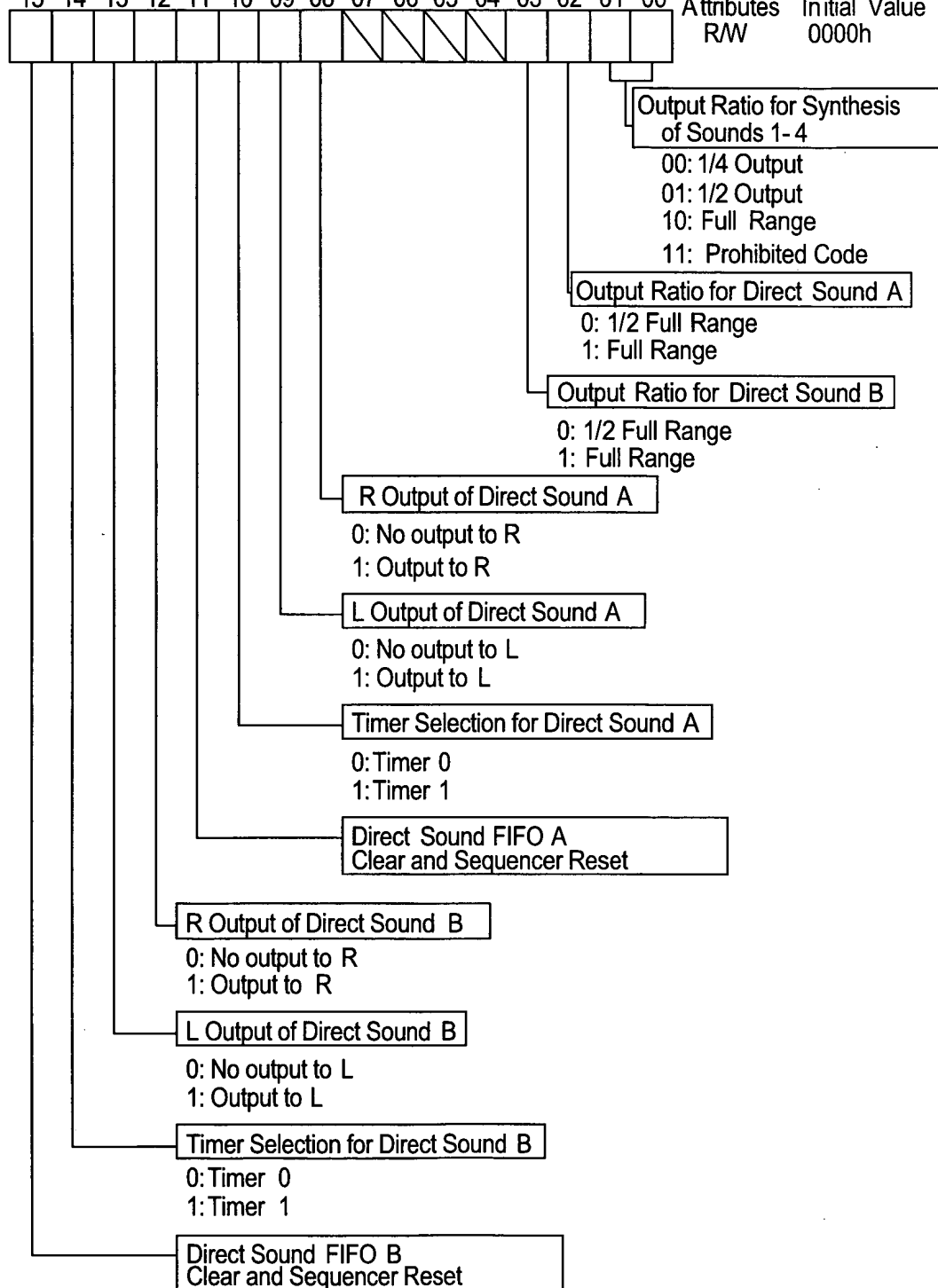


Fig. 78B

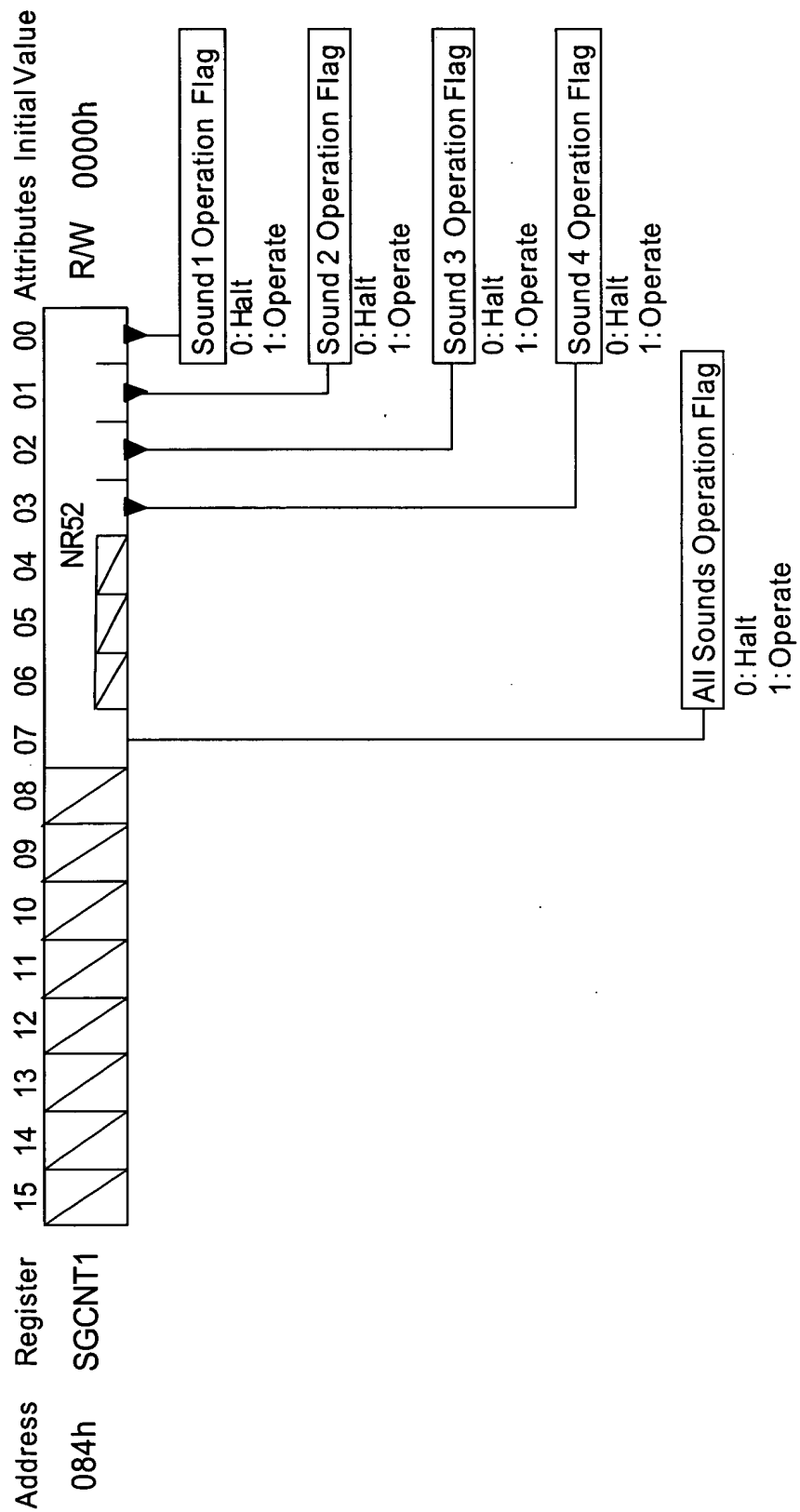


Fig. 78C

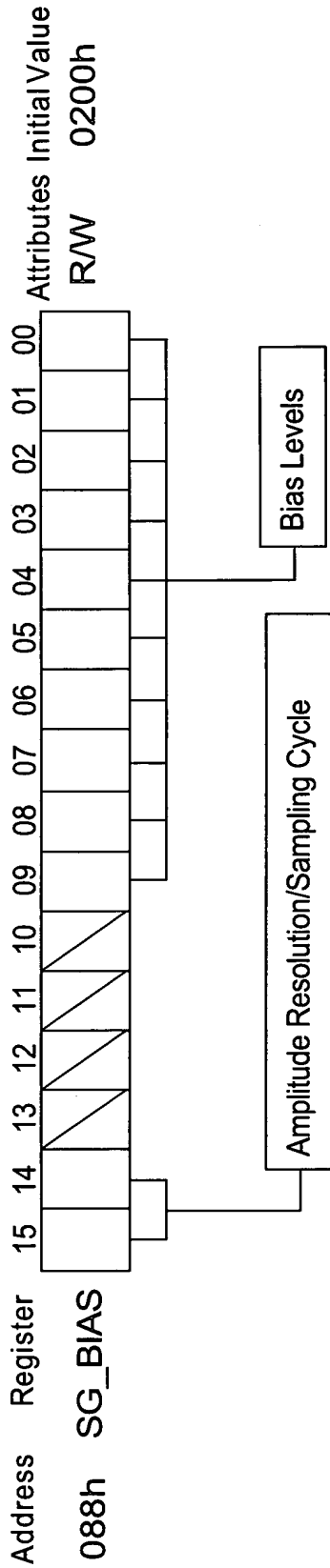


Fig. 79

Input Waveform(Waveform
Composition for All Sounds)

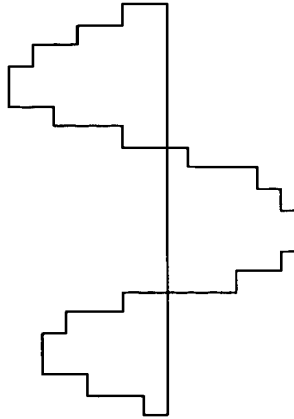
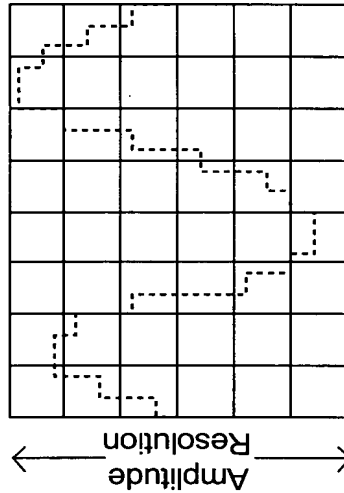


Fig. 80A

PWM Modulation



Time Base Resolution
(Sampling Frequency)

Fig. 80B

CPU Output Waveform

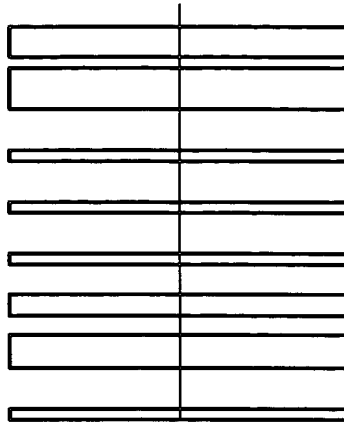


Fig. 80C

[illegible]

Fig. 81A

- ## 2) Timer Control

Fig. 81B

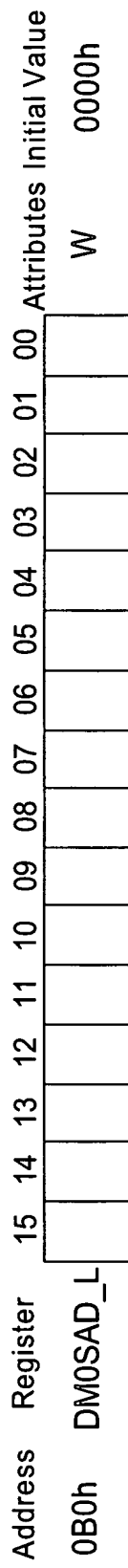


Fig. 82A

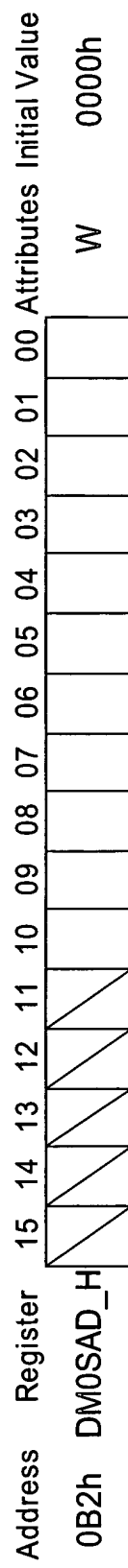


Fig. 82B

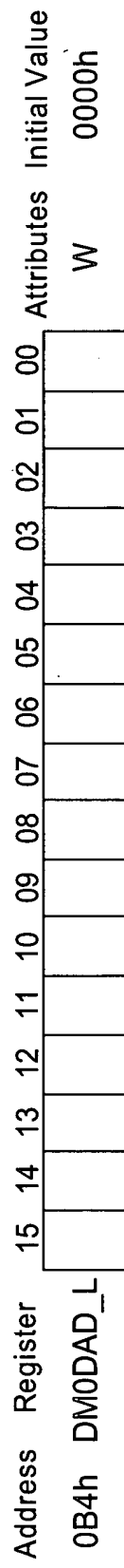


Fig. 83A

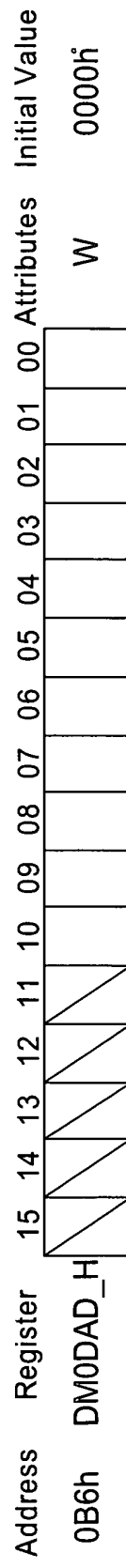


Fig. 83B

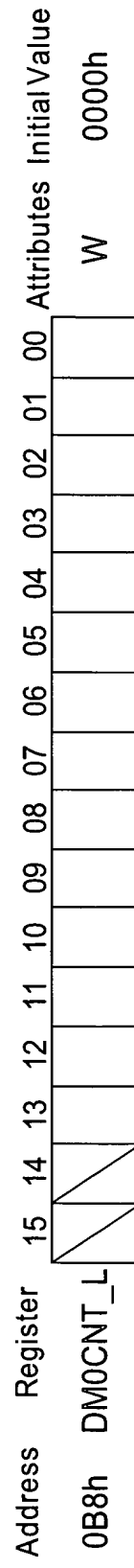


Fig. 84

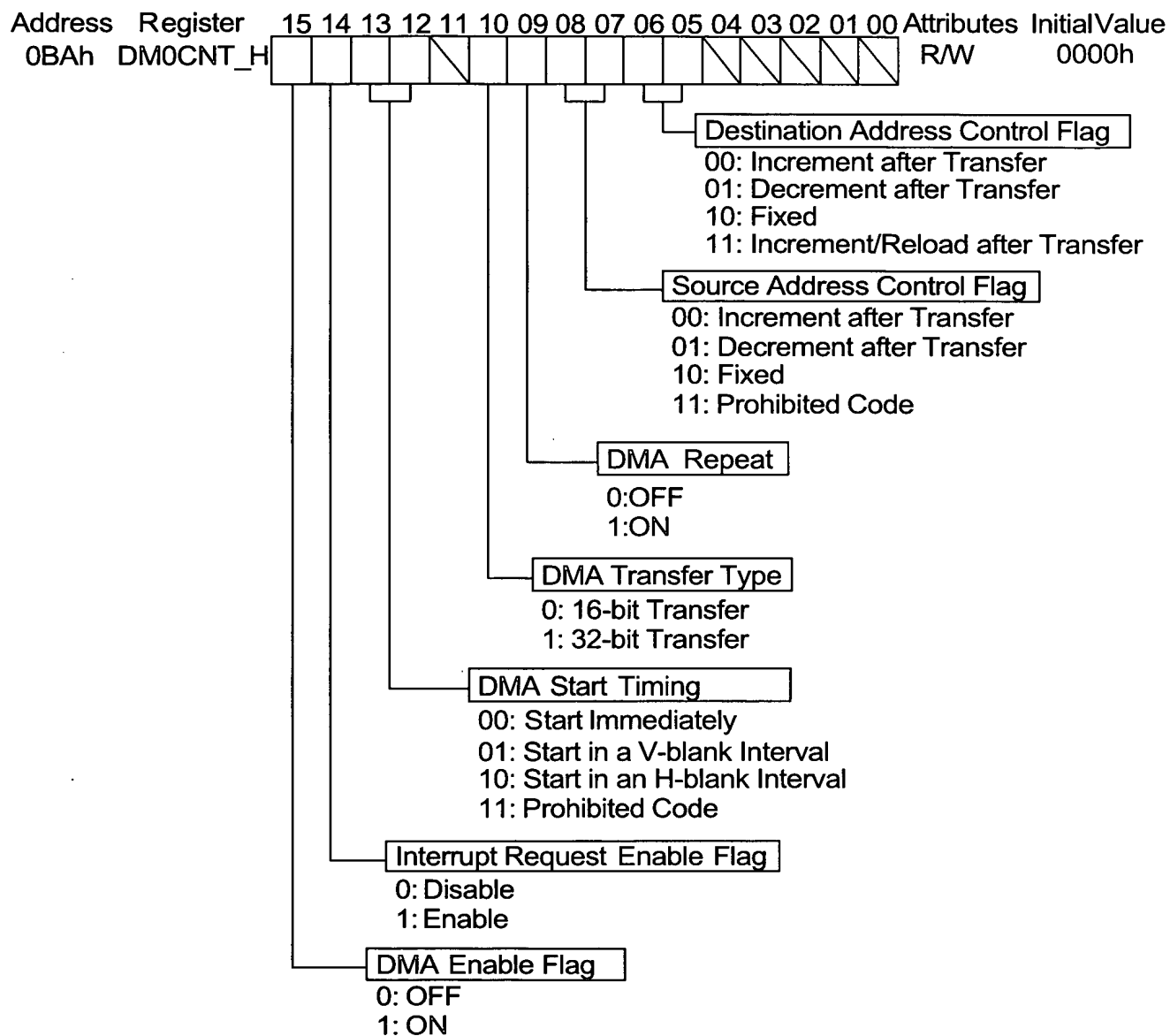


Fig. 85

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0BCh	DM1SAD_L																	W	0000h
0C8h	DM2SAD_L																		

Fig. 86A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0BEh	DM1SAD_H																	W	0000h
0CAh	DM2SAD_H																		

Fig. 86B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C0h	DM1DAD_L																	W	0000h
0CCh	DM2DAD_L																		

Fig. 87A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C2h	DM1DAD_H																	W	0000h
0CEh	DM2DAD_H																		

Fig. 87B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C4h	DM1CNT_L																	W	0000h
0D0h	DM2CNT_L																		

Fig. 88

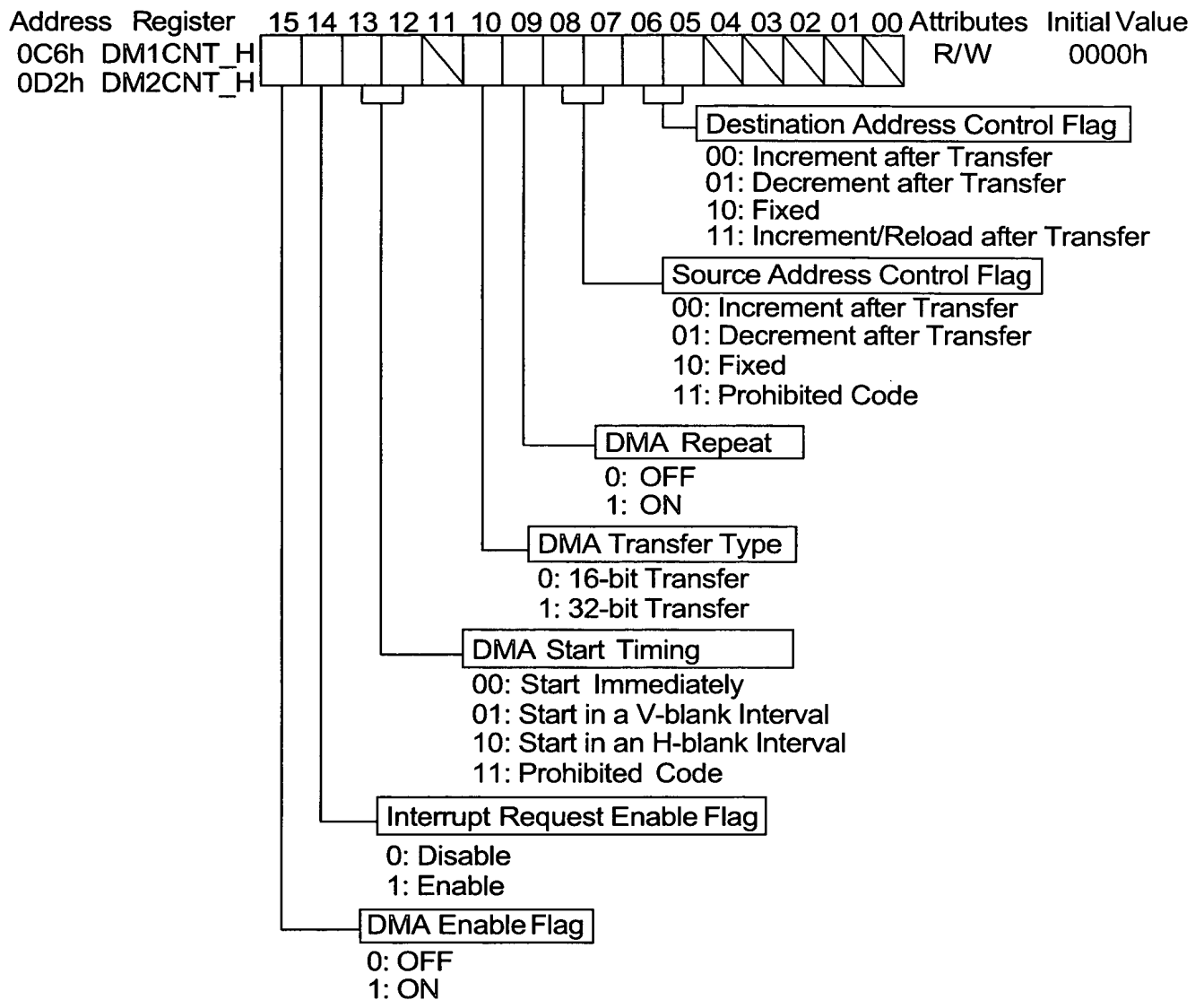


Fig. 89

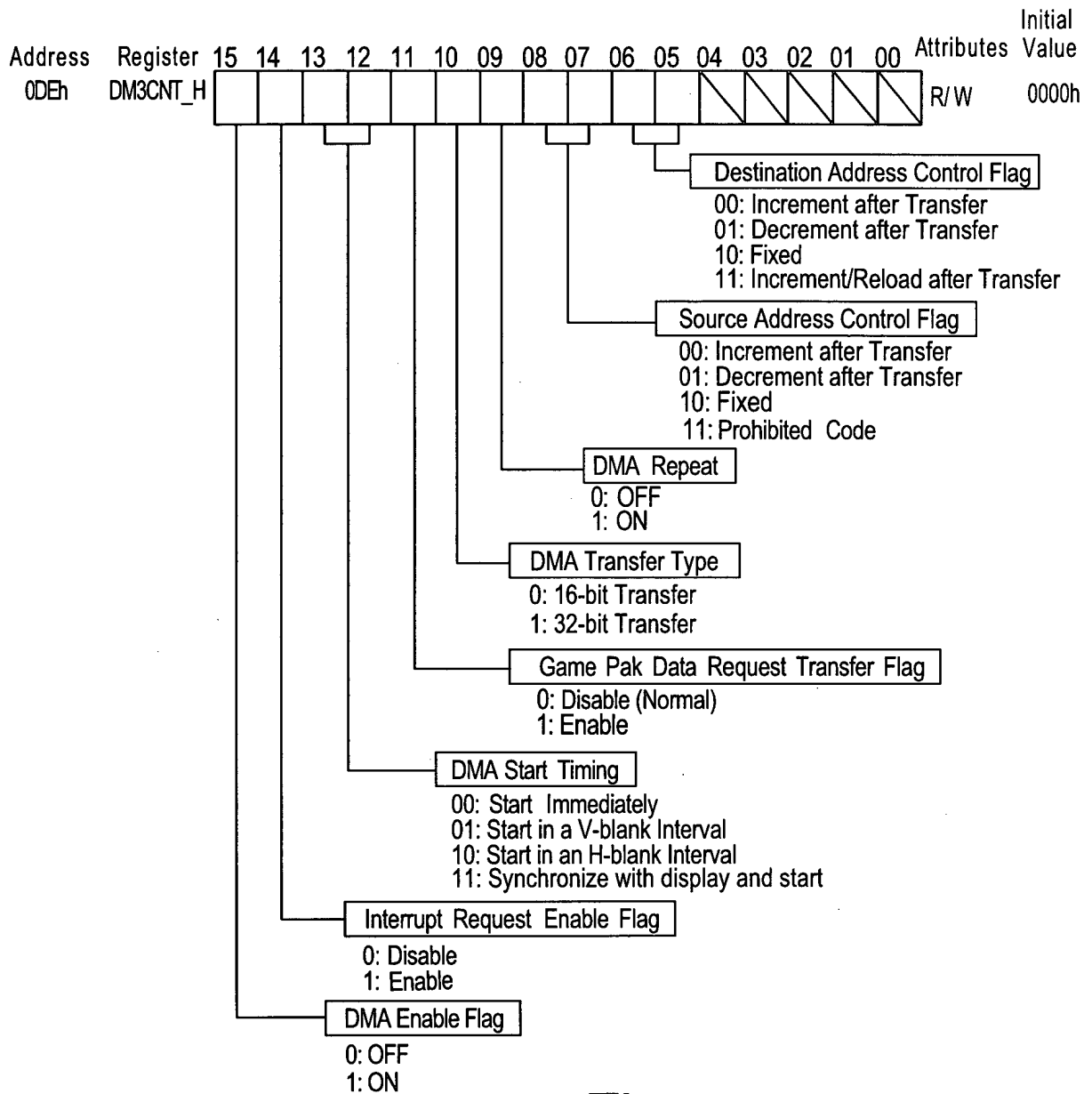


Fig. 93

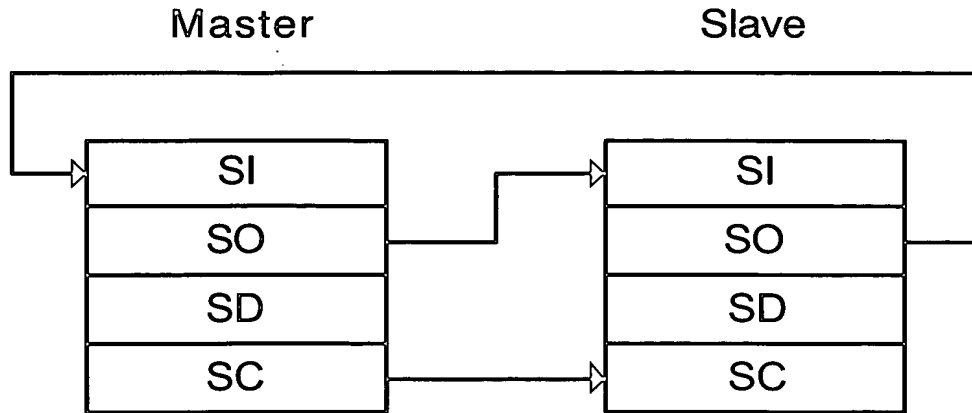


Fig. 94



Fig. 95A

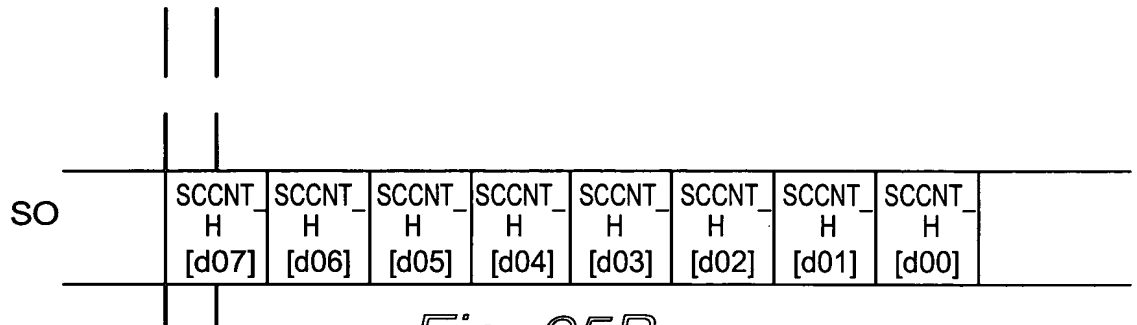


Fig. 95B

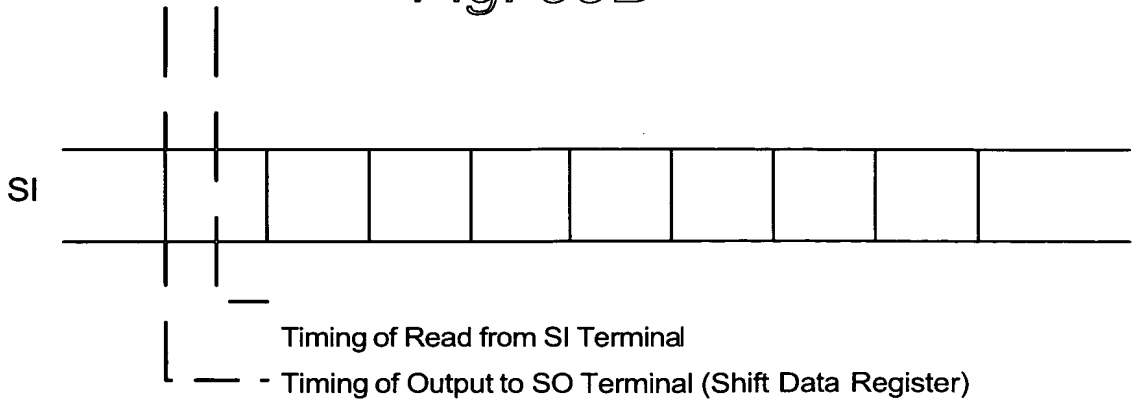


Fig. 95C

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
12A h	SCCNT_H																	R/W	0000h

Fig. 96

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
120h	SCD0	Data 0																R/W	0000h

Fig. 97A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
122h	SCD1	Data 1																R/W	0000h

Fig. 97B

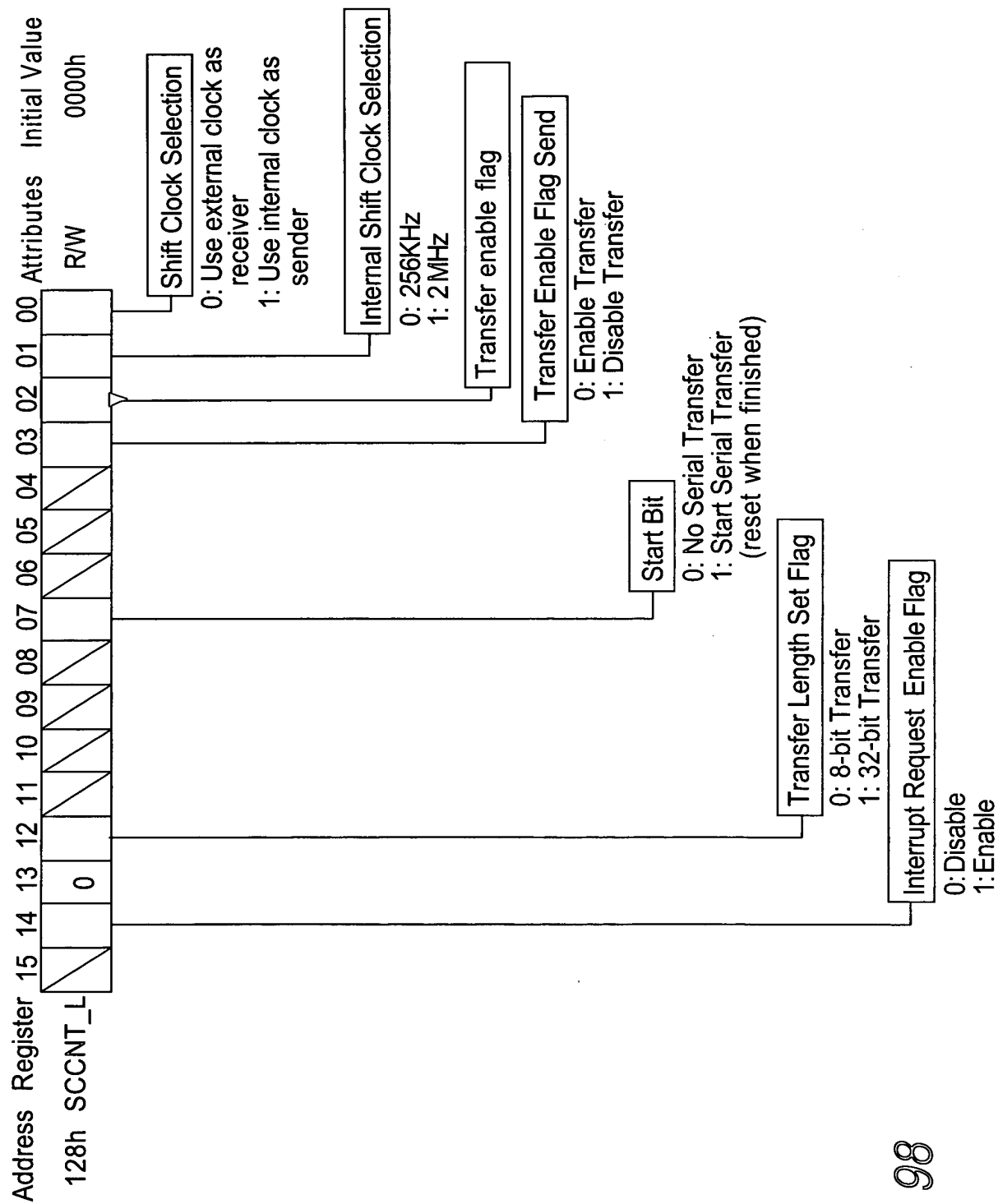
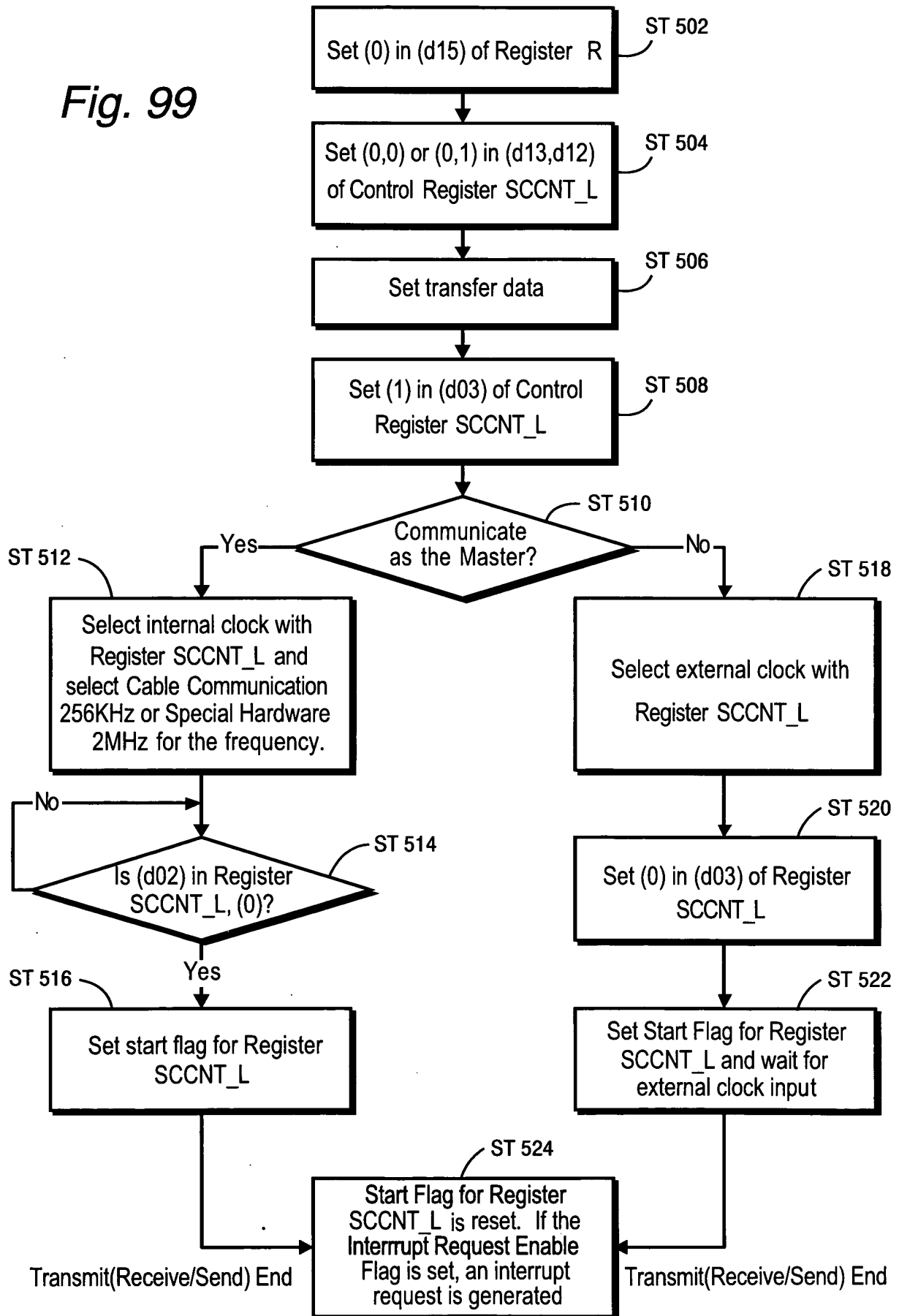


Fig. 8

Fig. 99



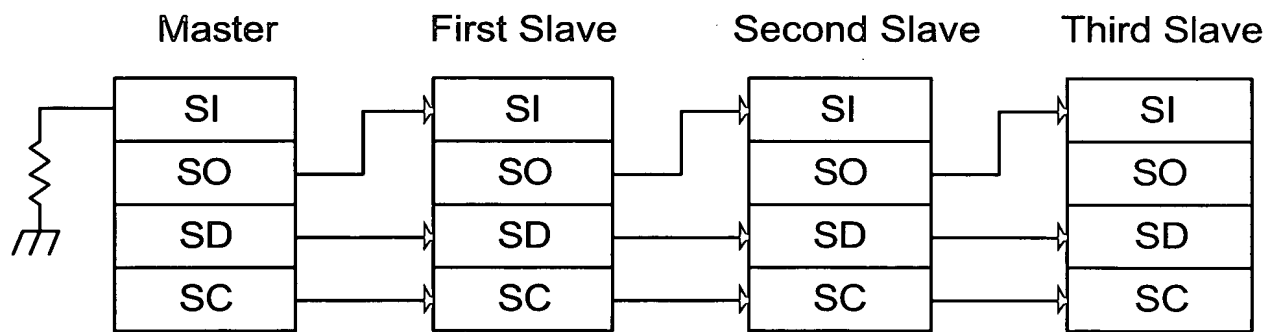


Fig. 100

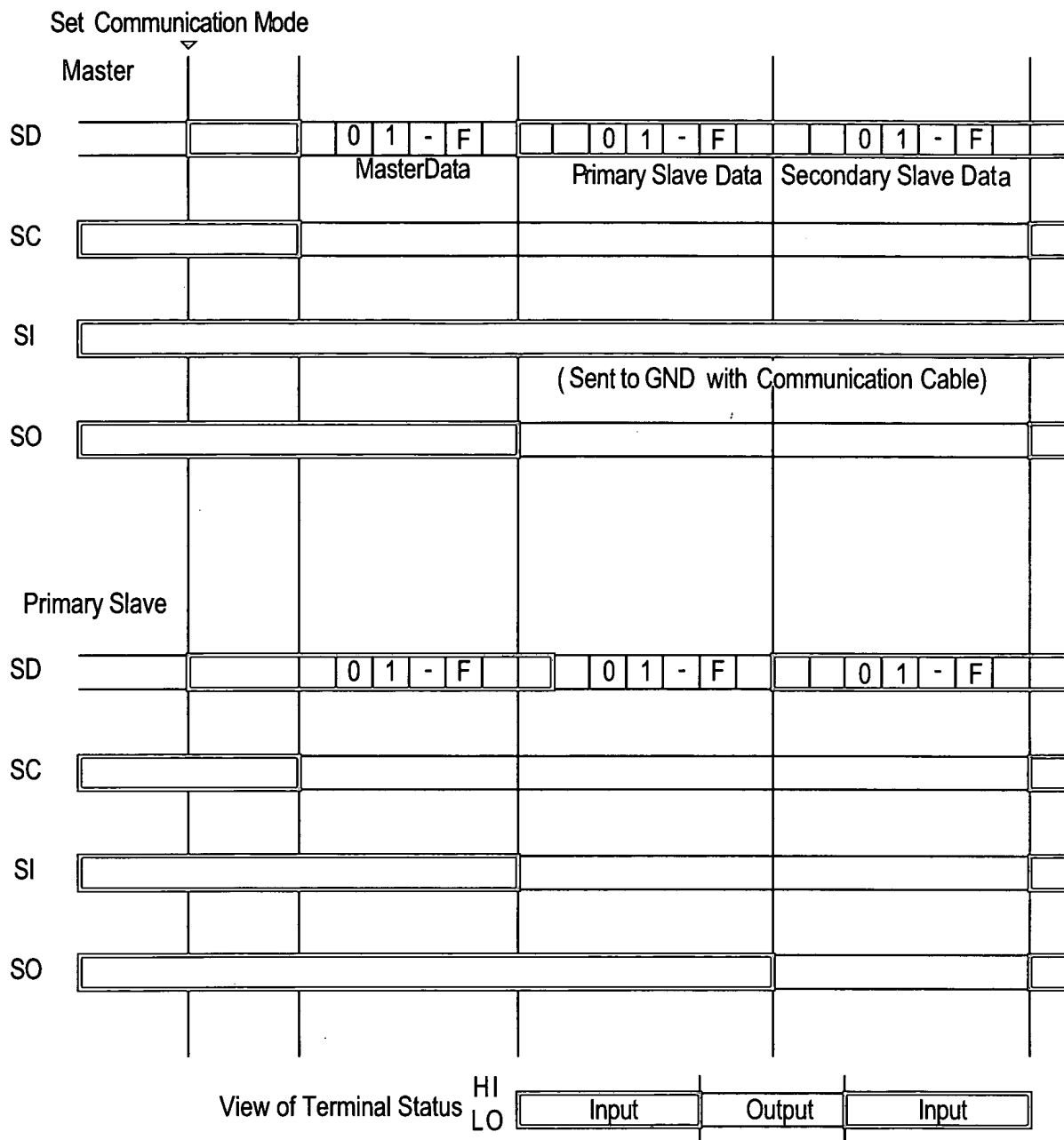


Fig. 101

Multi Player Communication Cable Connecting Diagram

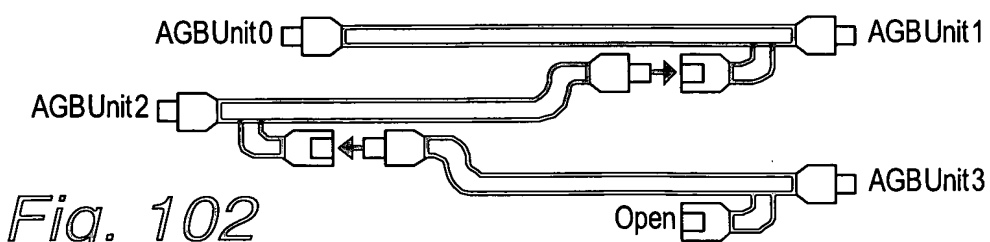


Fig. 102

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
12Ah	SCCNT_H																	R/W	0000h

Fig. 103

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
120h	SCD0	Data 0																R/W	0000h

Fig. 104A

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
122h	SCD1	Data 1																R/W	0000h

Fig. 104B

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
124h	SCD2	Data 2																R/W	0000h

Fig. 104C

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
126h	SCD3	Data 3																R/W	0000h

Fig. 104D

00000000 00000000 00000000 00000000

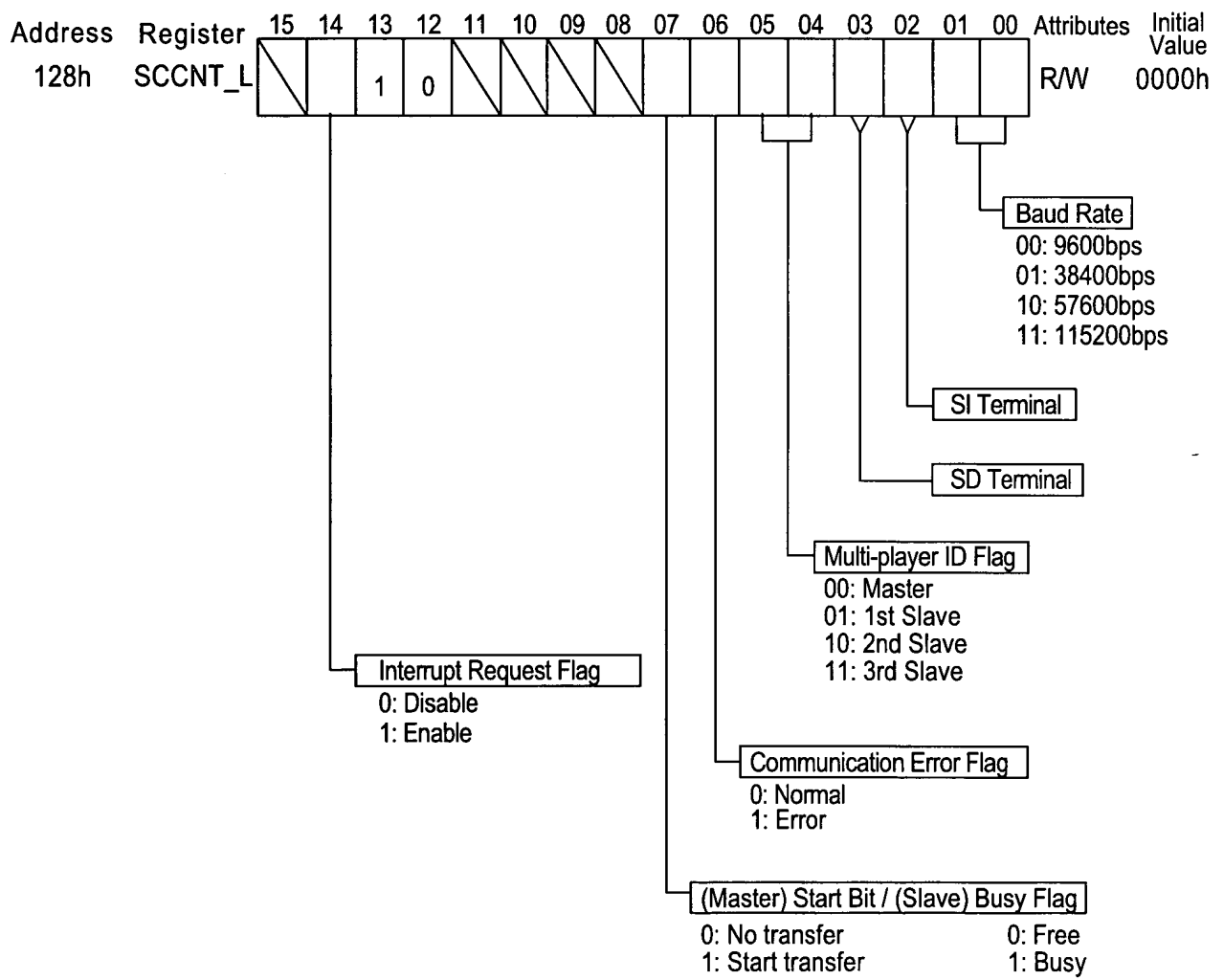


Fig.105

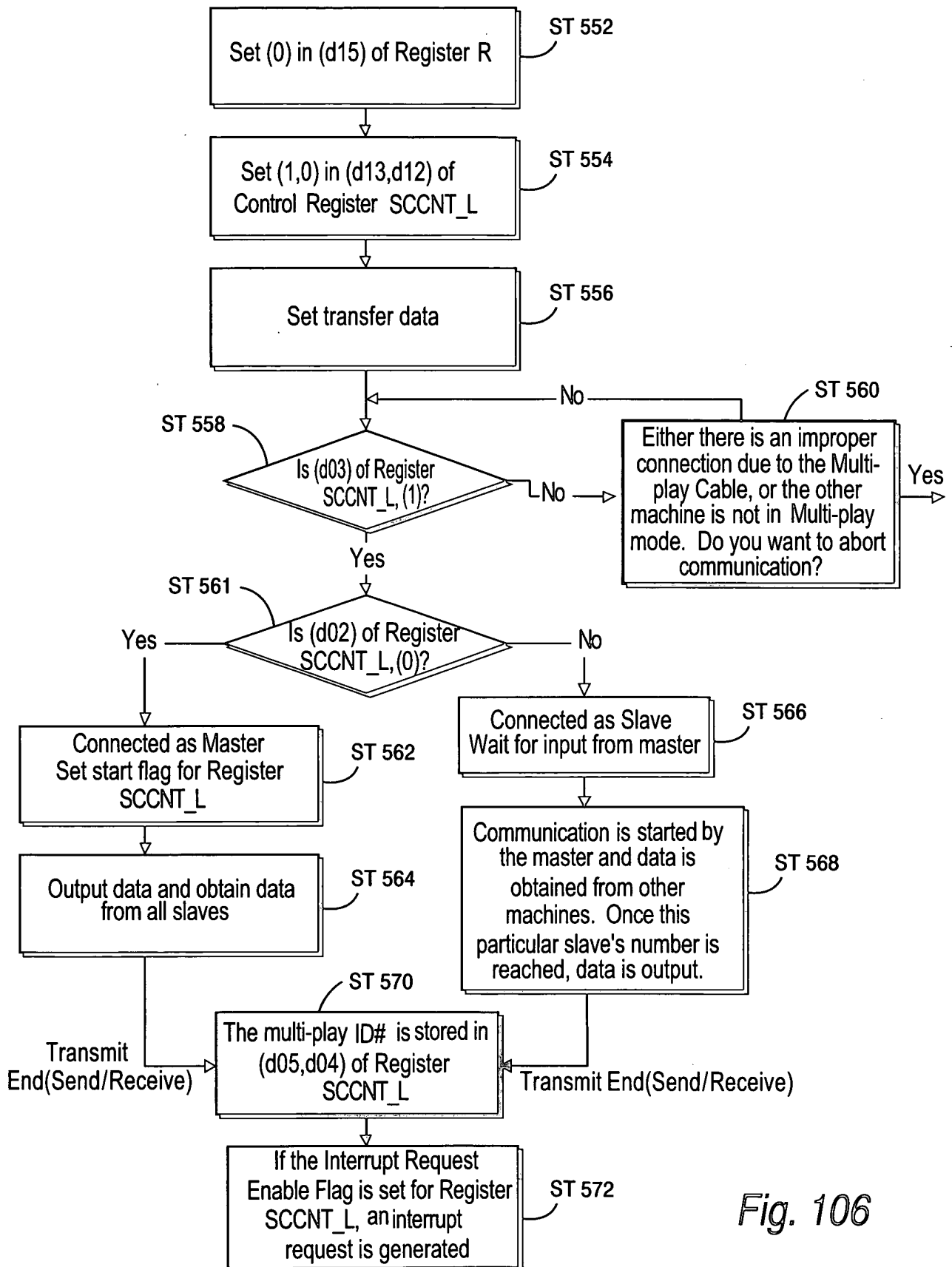


Fig. 106

UART Communication

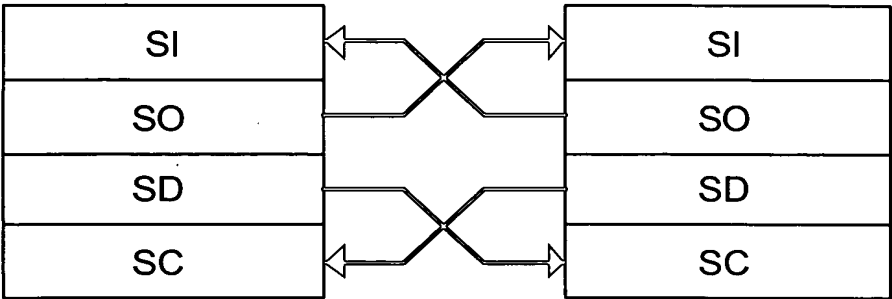


Fig. 107

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
12Ah	SCCNT_H																	R/W	0000h

Fig. 108A

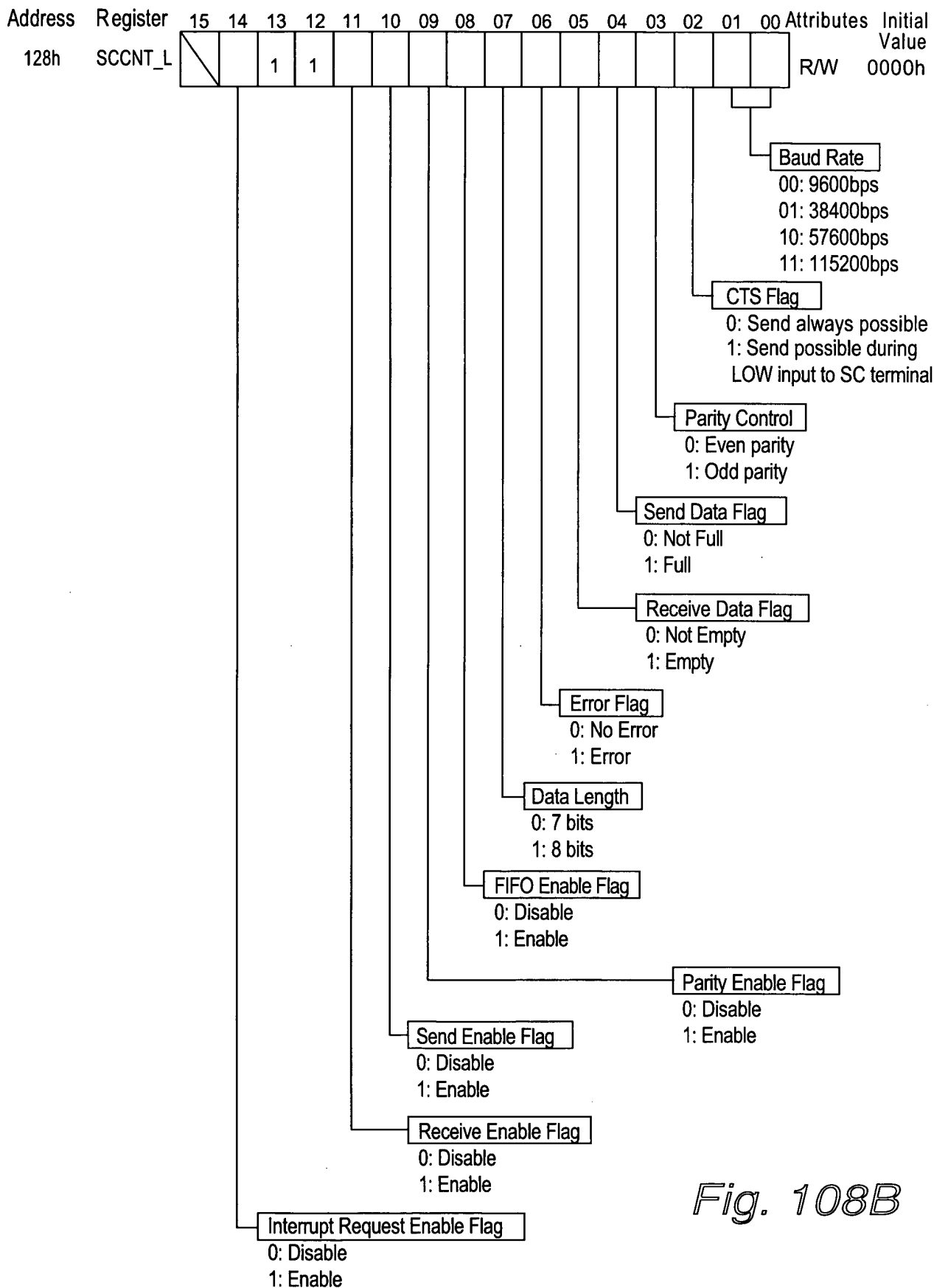


Fig. 108B

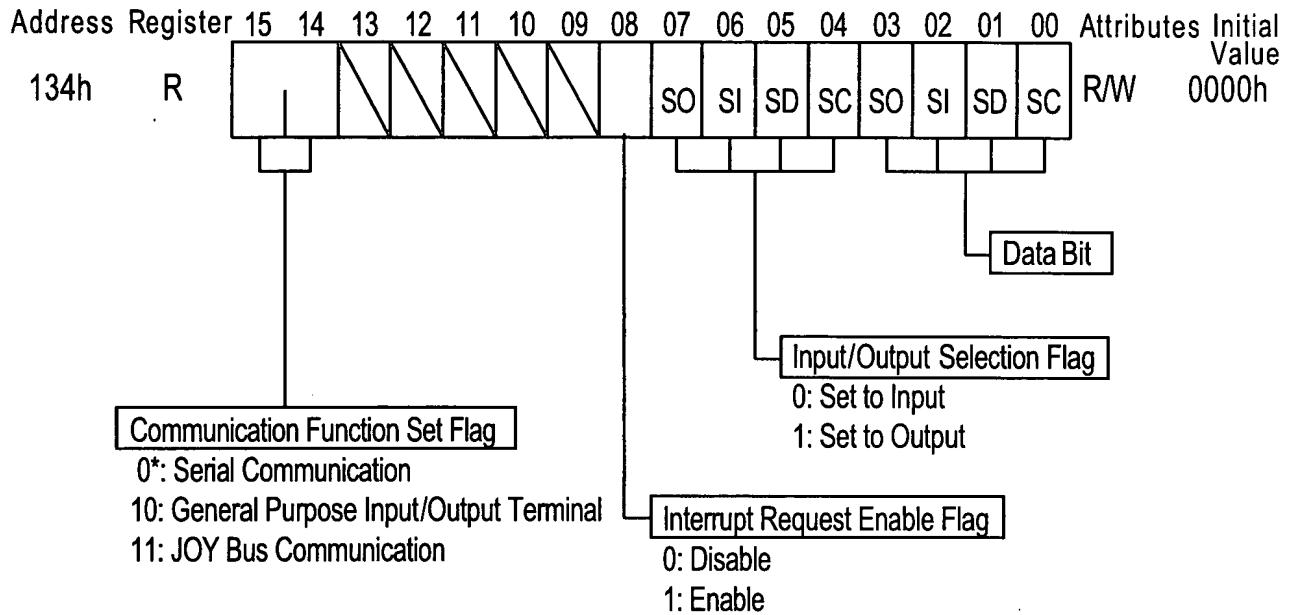


Fig. 109

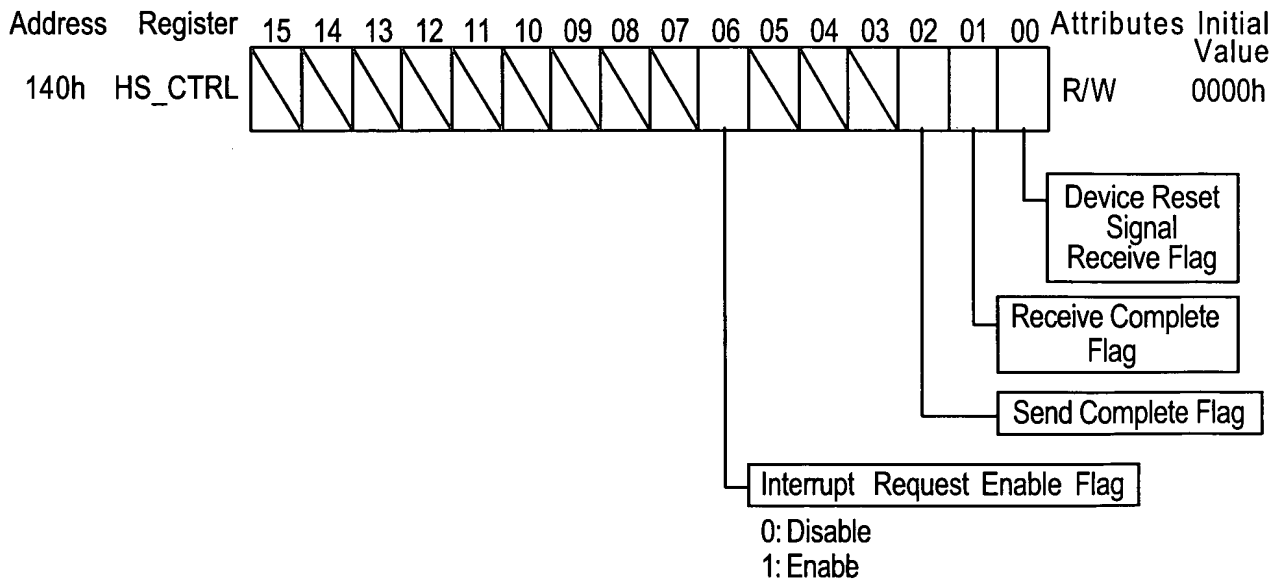


Fig. 110

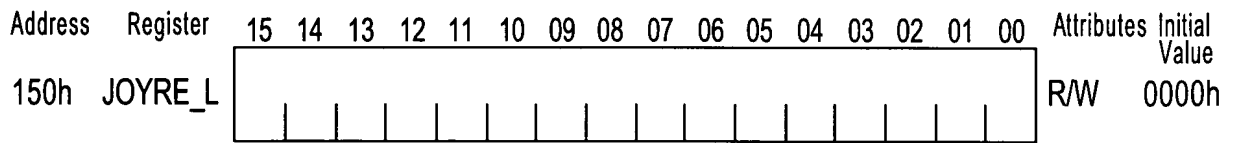


Fig. 111A

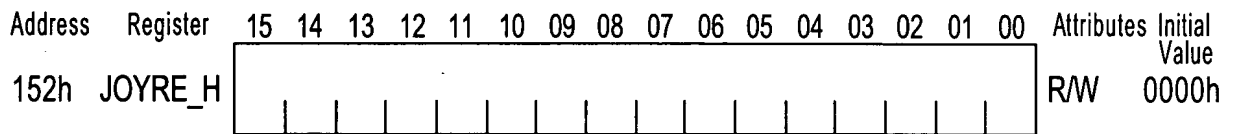


Fig. 111B

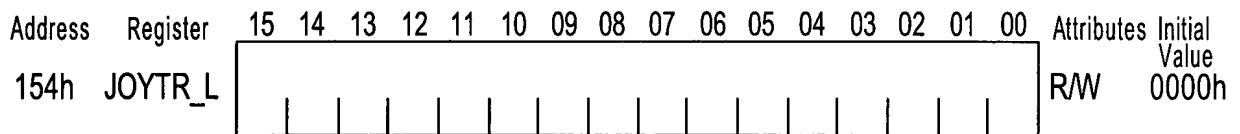


Fig. 112A

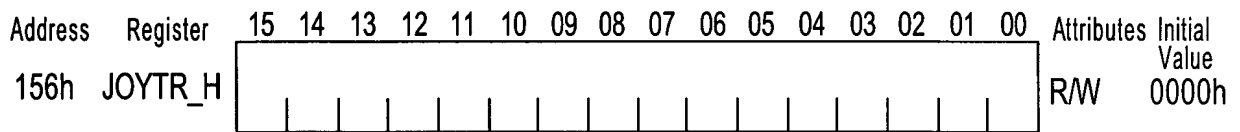


Fig. 112B

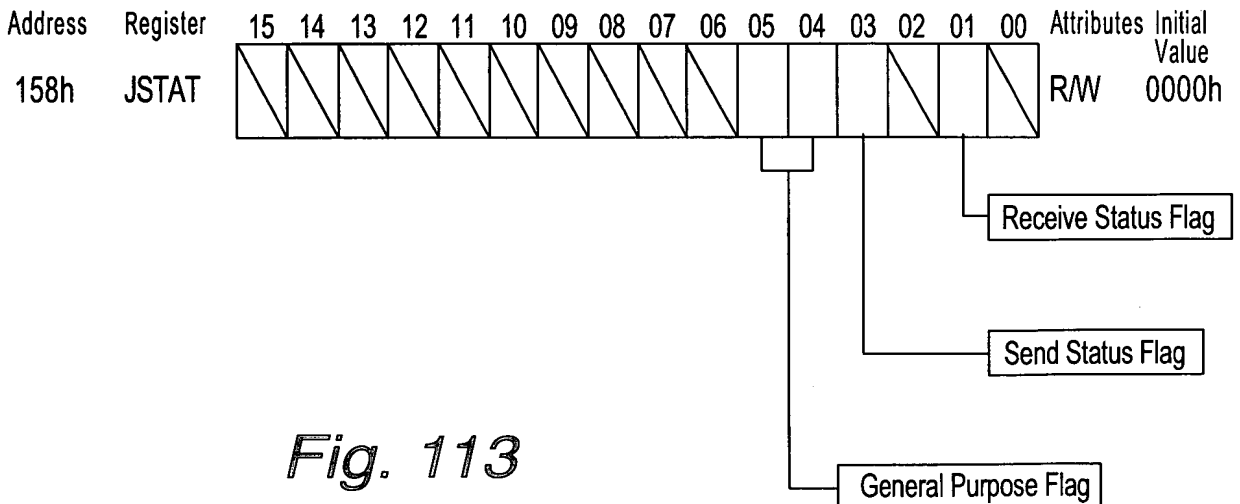


Fig. 113

0000000000000000

Device Reset

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	1	1	1	1	1	1	1	1	Command 255(FFh)
Send	1	0	0	0	0	0	0	0	0	Type Number 0400h
	2	0	0	0	0	0	1	0	0	
	3	Lower 8 bits of Register JSTAT								Communication Status

Fig. 114

Type/Status Data Request

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	0	0	0	0	0	Command 0(00h)
Send	1	0	0	0	0	0	0	0	0	Type Number 0400h
	2	0	0	0	0	0	1	0	0	
	3	Lower 8 bits of Register JSTAT								Communication Status

Fig. 115

[illegible][illegible]

Fig. 116

AGB Data Read

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	1	0	1	0	0	Command 20(14h)
Send	2	Lower 8 bits of send data Register JOYTR_L								Send Data
	3	Upper 8 bits of send data Register JOYTR_L								
	4	Lower 8 bits of send data Register JOYTR_H								
	5	Upper 8 bits of send data Register JOYTR_H								
	6	Lower 8 bits of Register JSTAT								Communication Status

Fig. 117

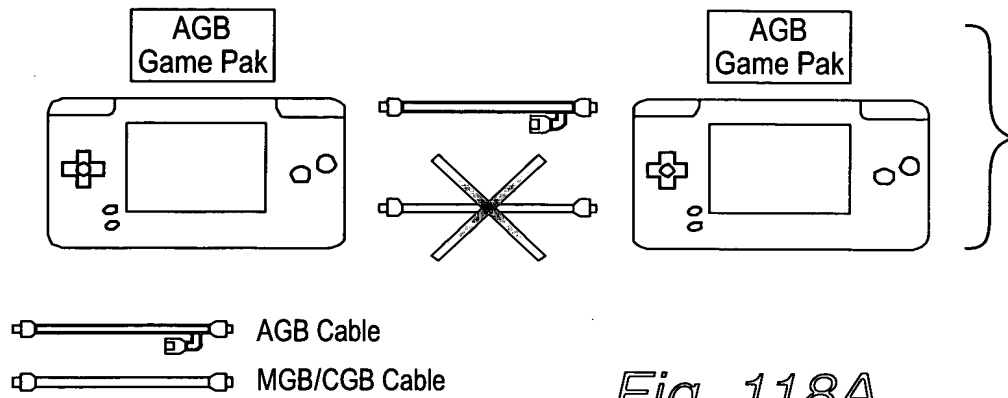


Fig. 118A

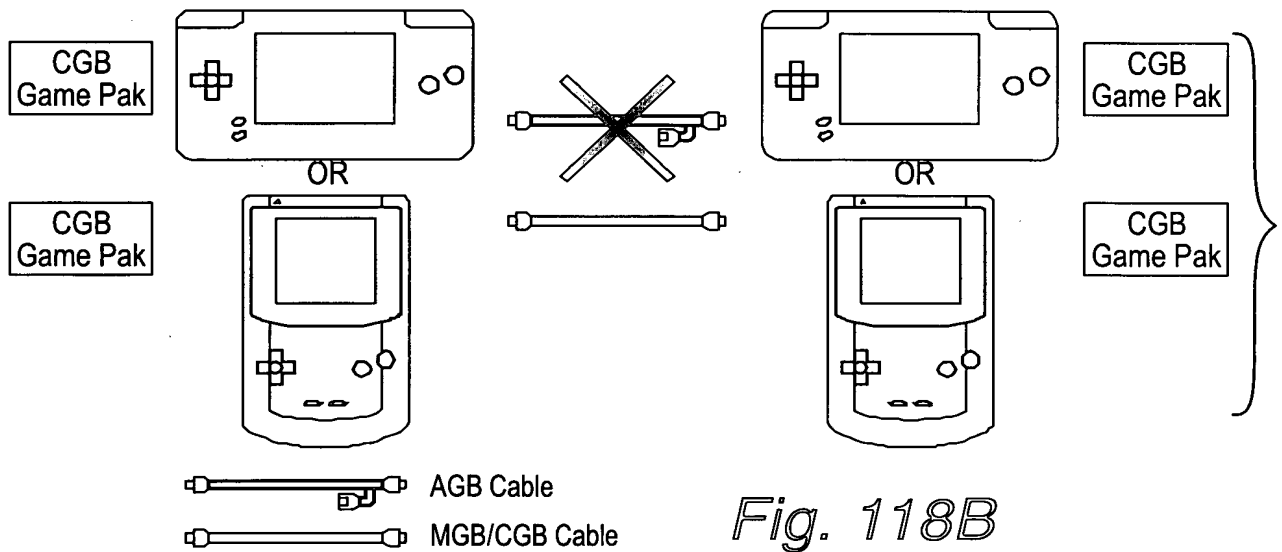


Fig. 118B

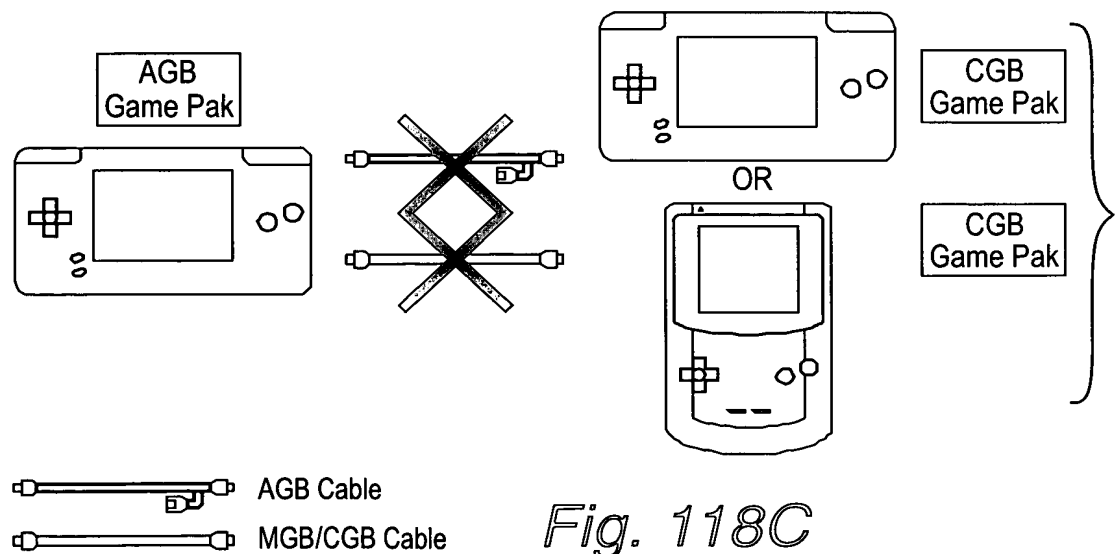
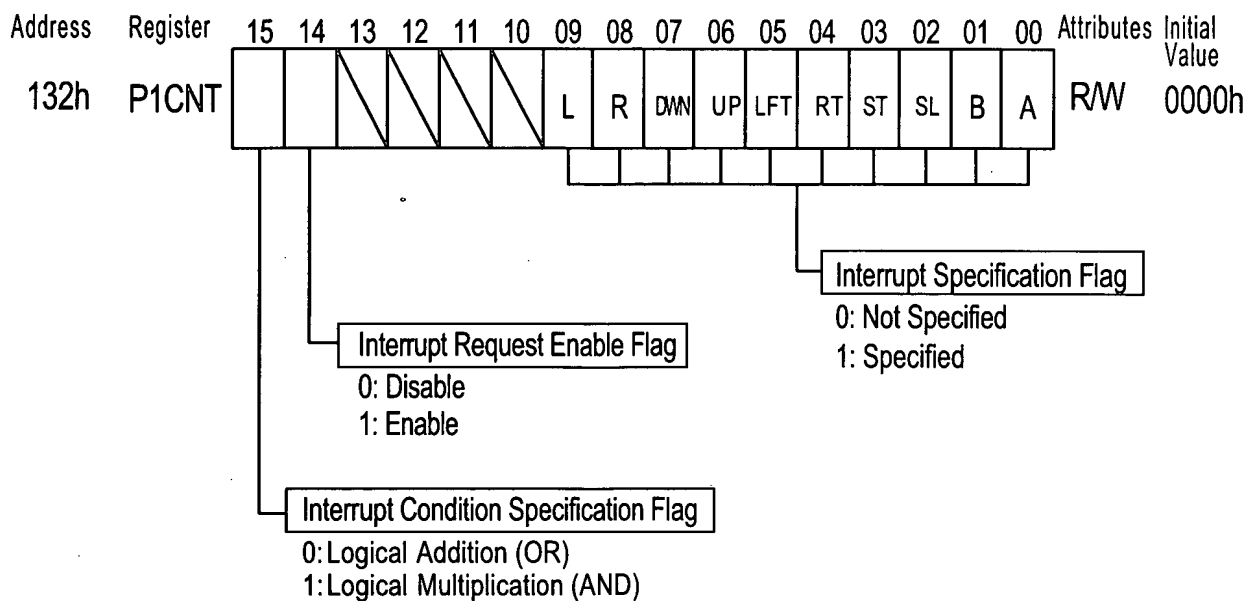
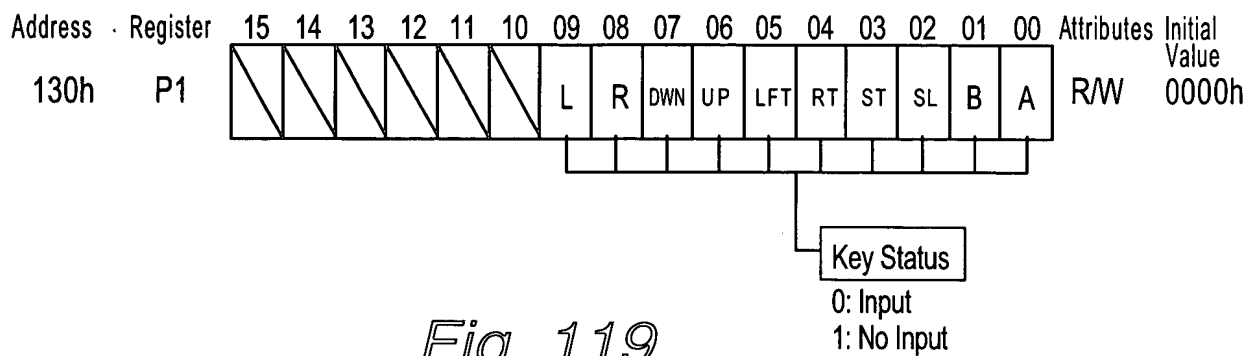


Fig. 118C



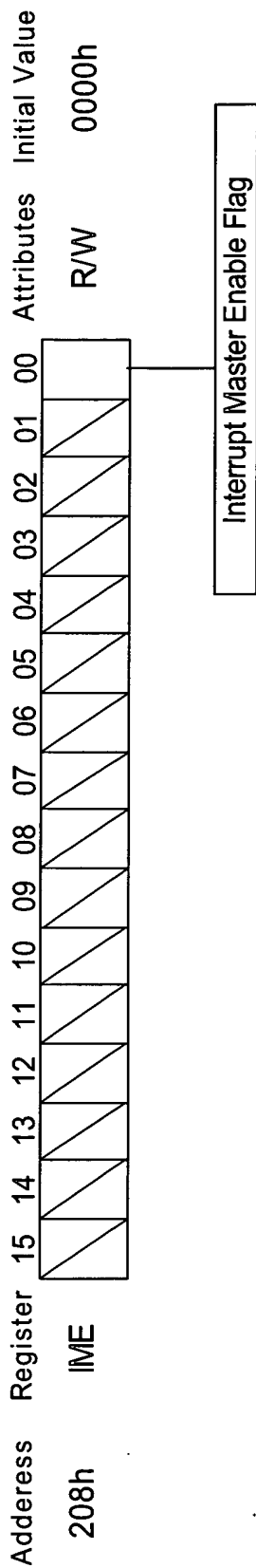


Fig. 121

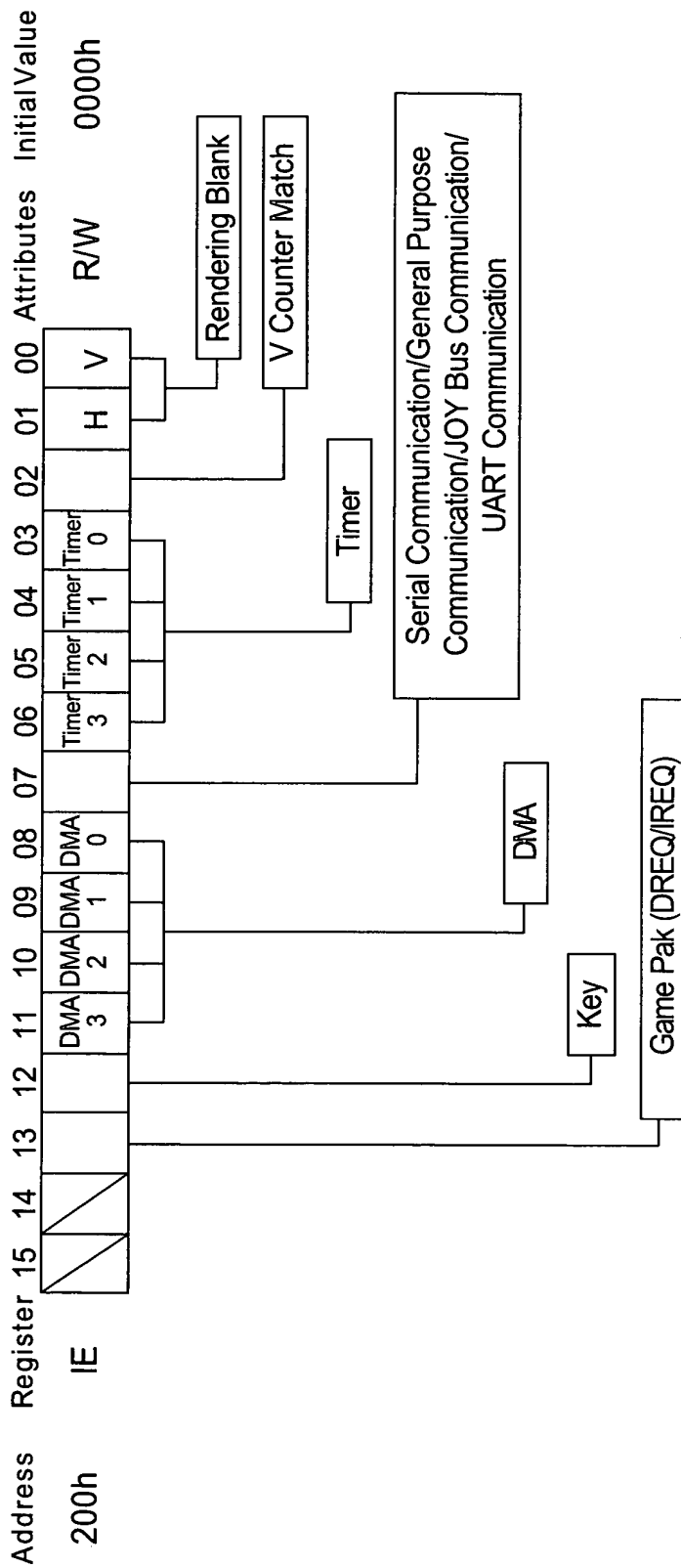


Fig. 122

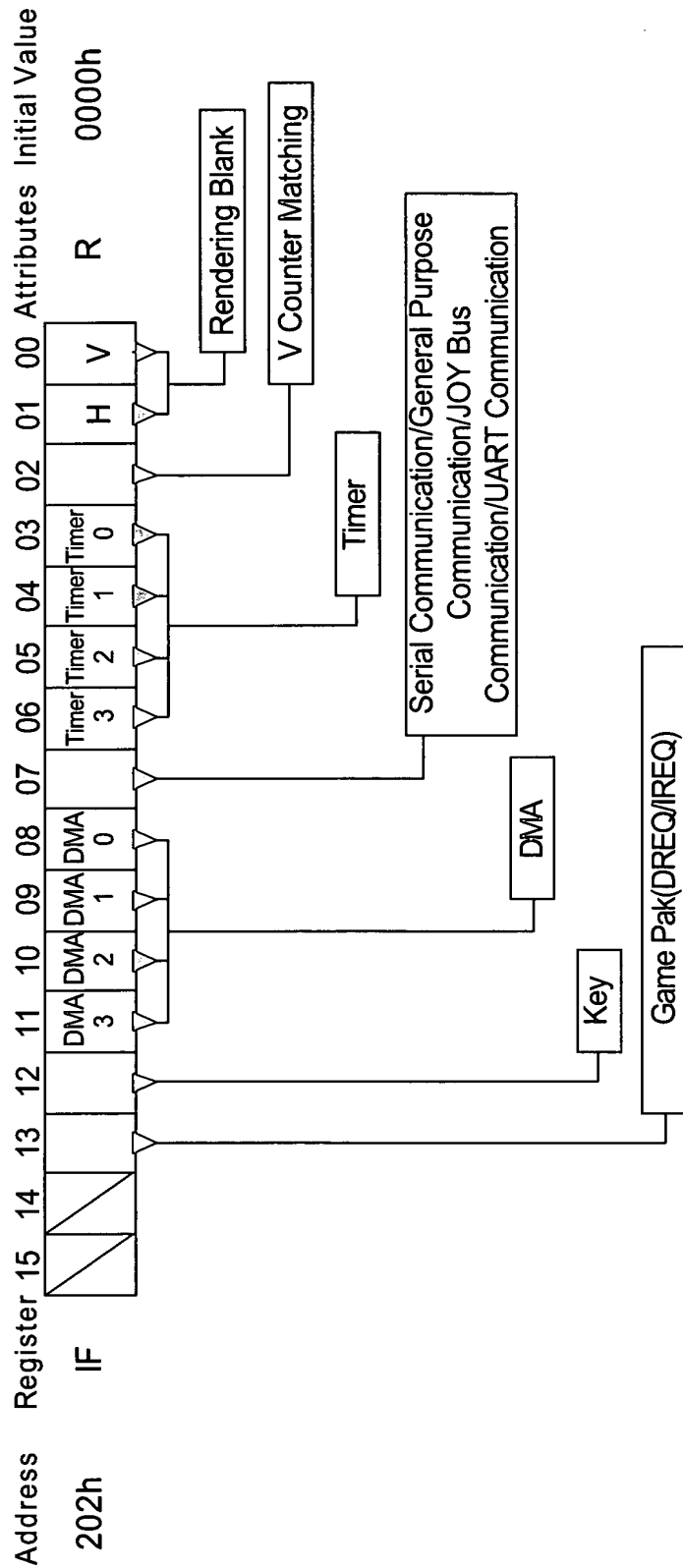


Fig. 123

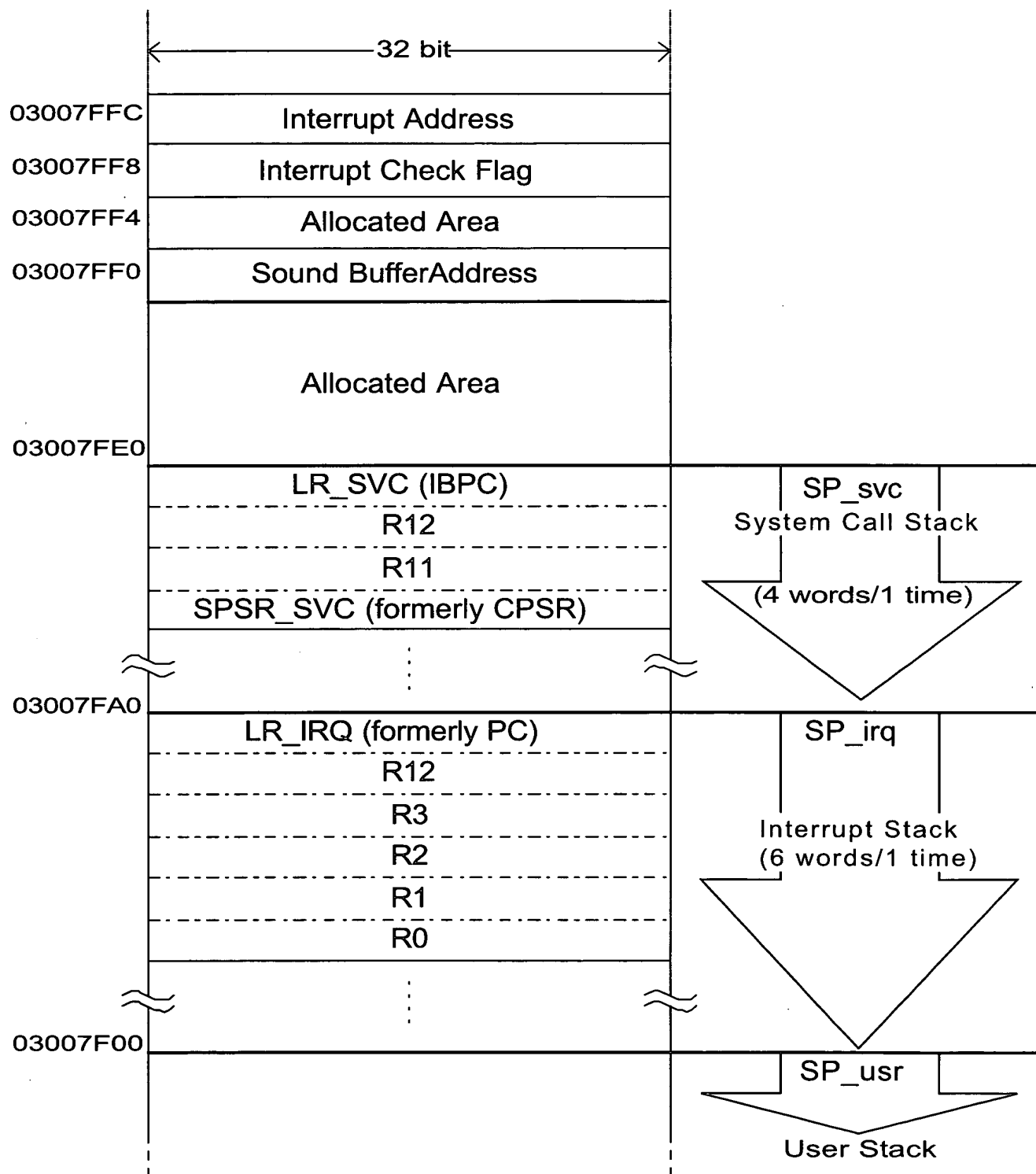


Fig. 124

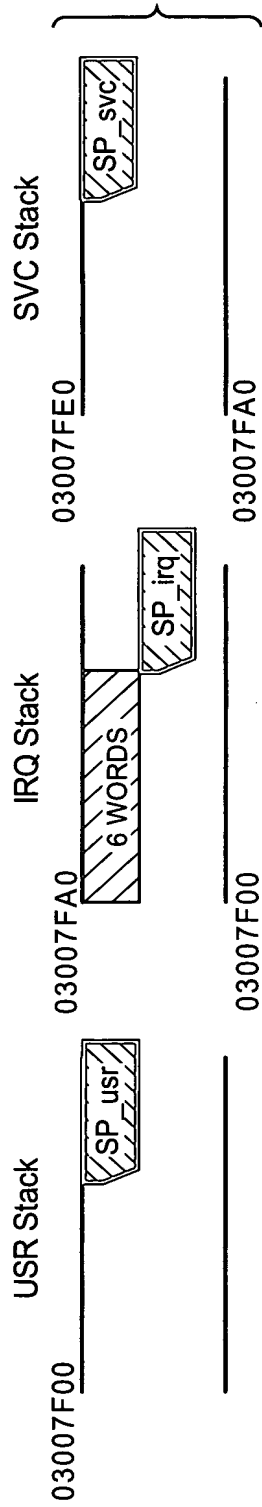


Fig. 125A

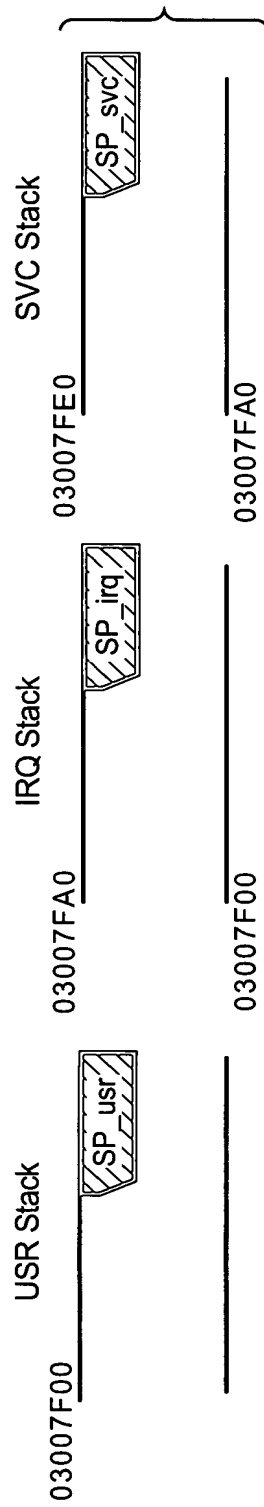


Fig. 125B

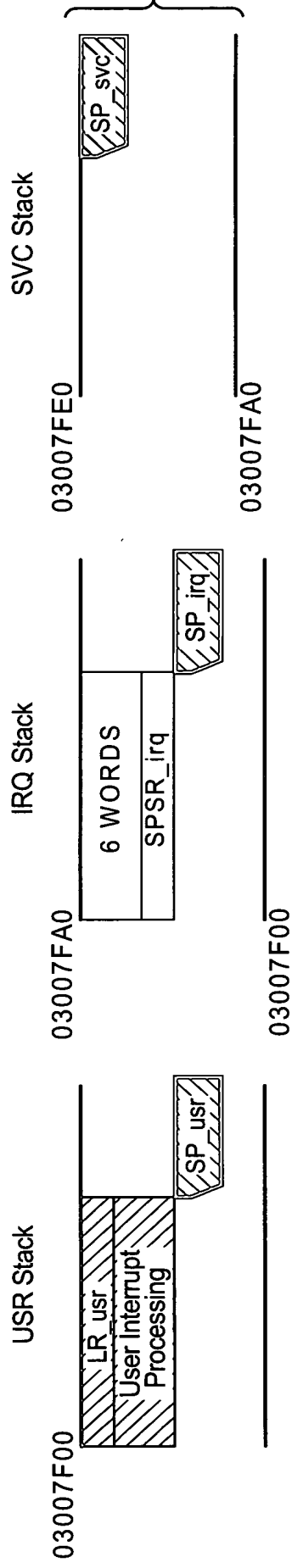


Fig. 126C

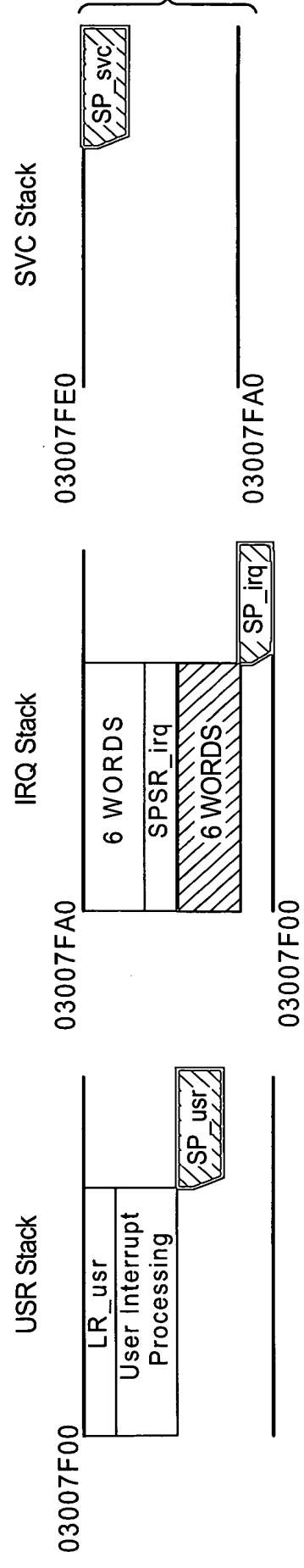


Fig. 126D

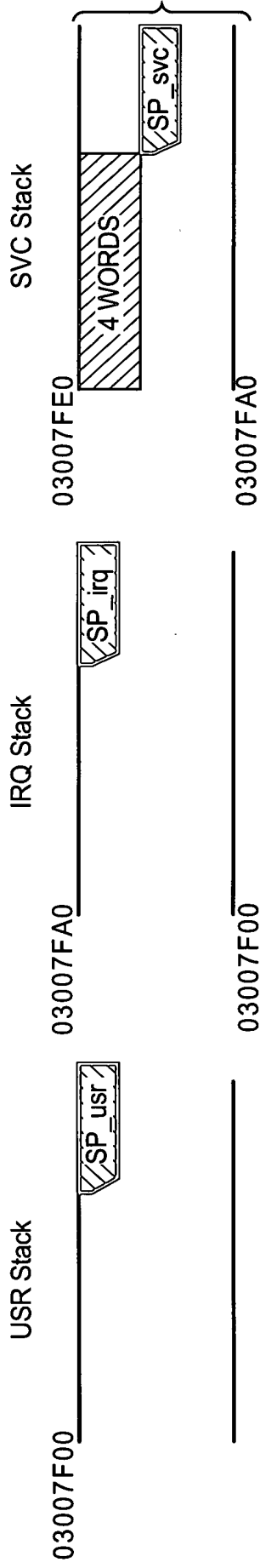


Fig. 127A

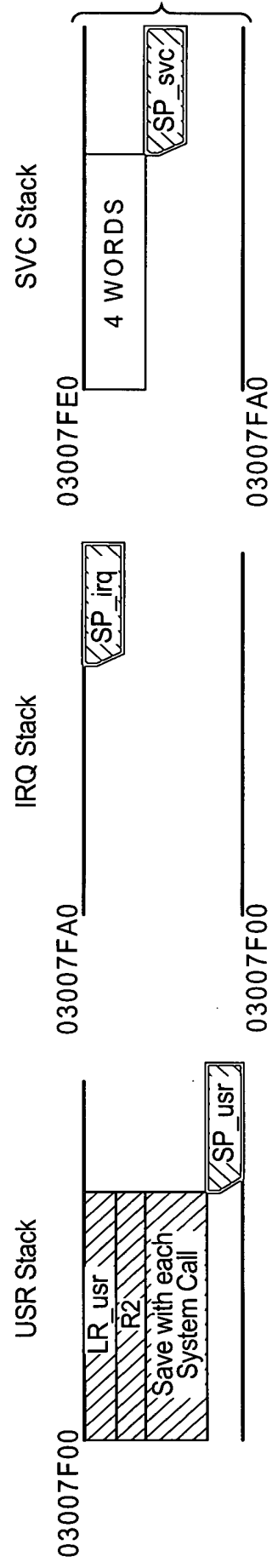


Fig. 127B

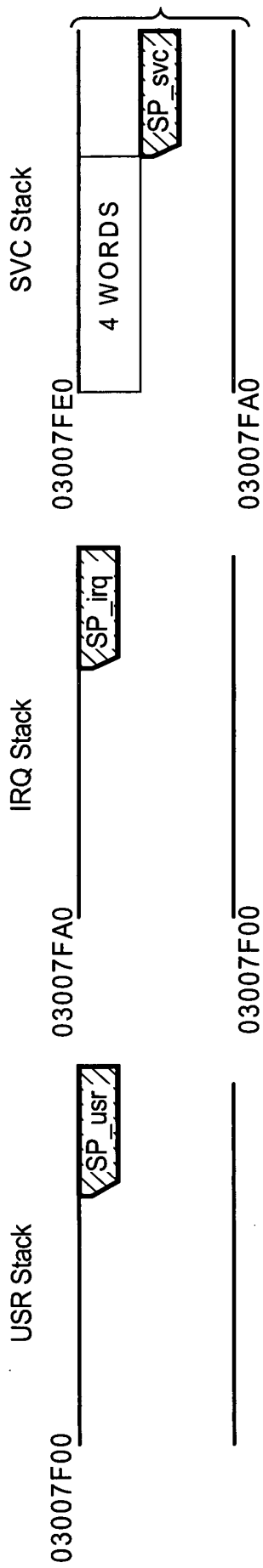


Fig. 127C

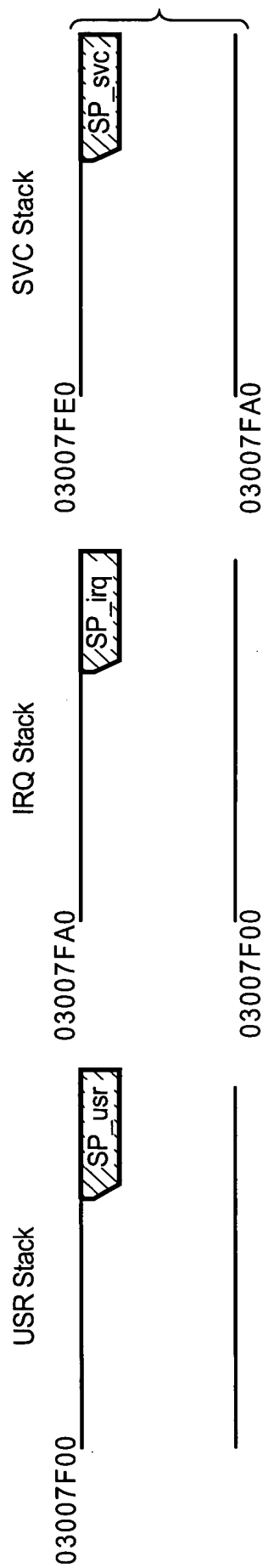


Fig. 127D

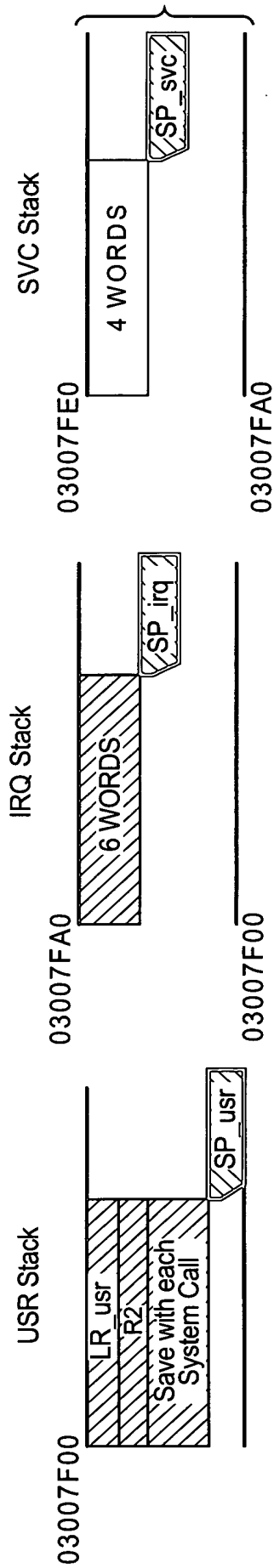


Fig. 128C

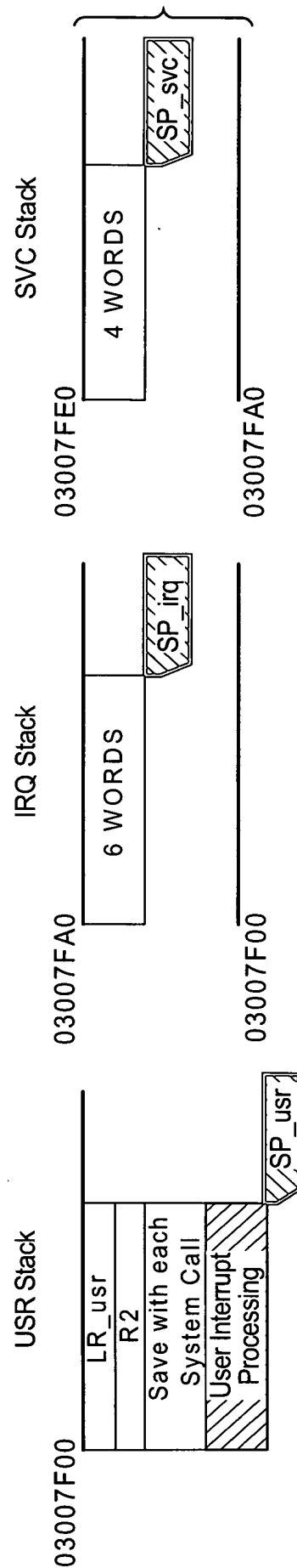


Fig. 128D

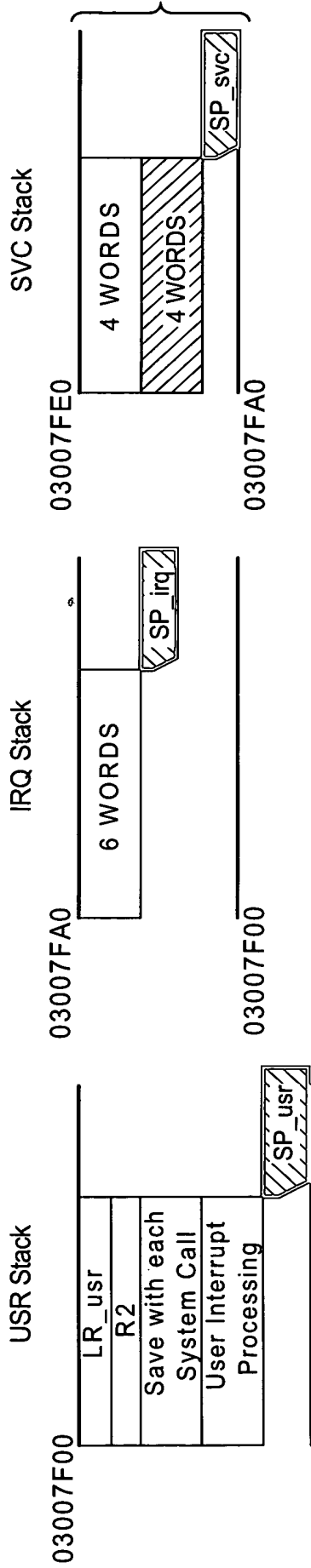


Fig. 128E

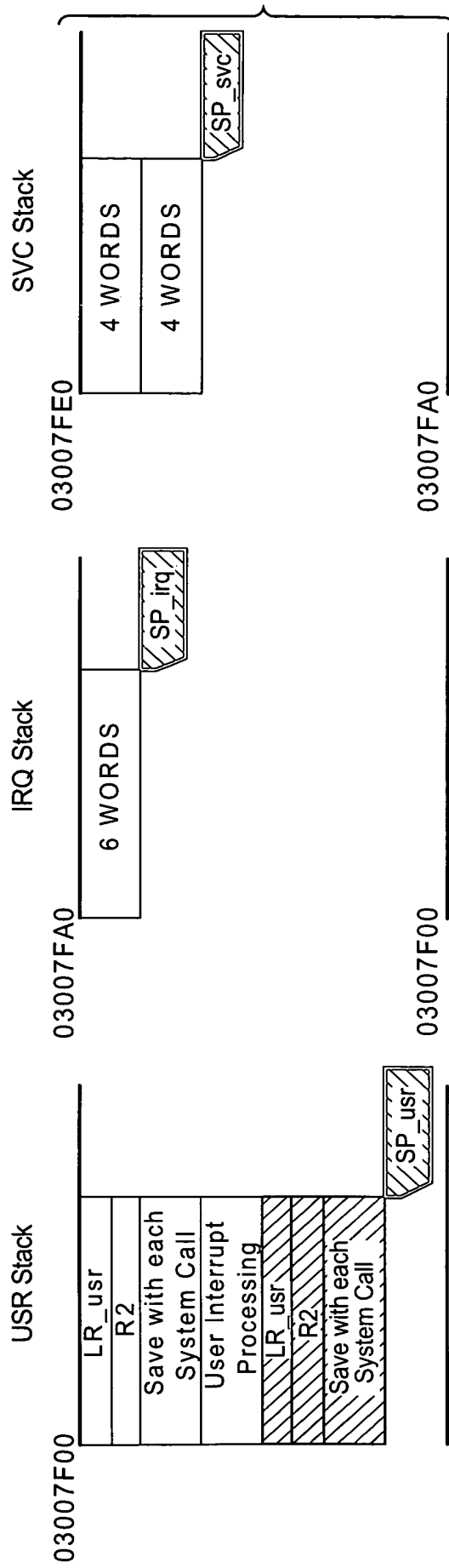


Fig. 128F

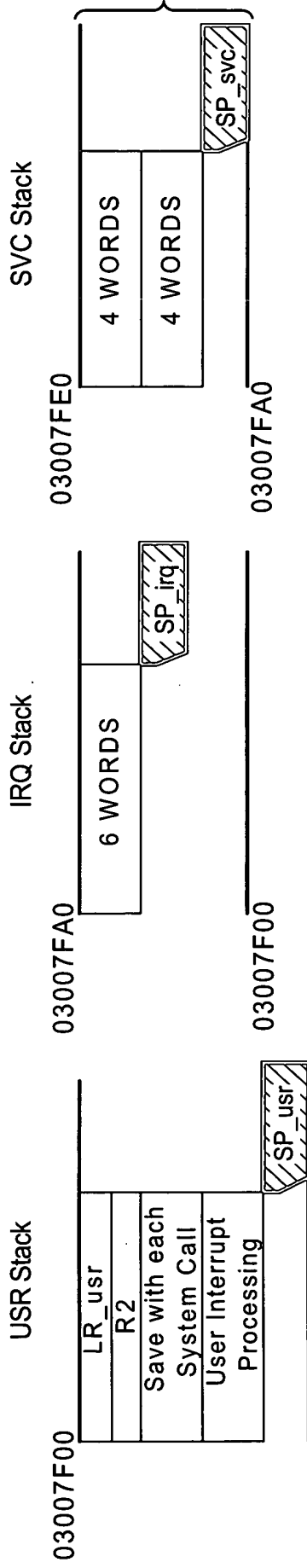


Fig. 128G

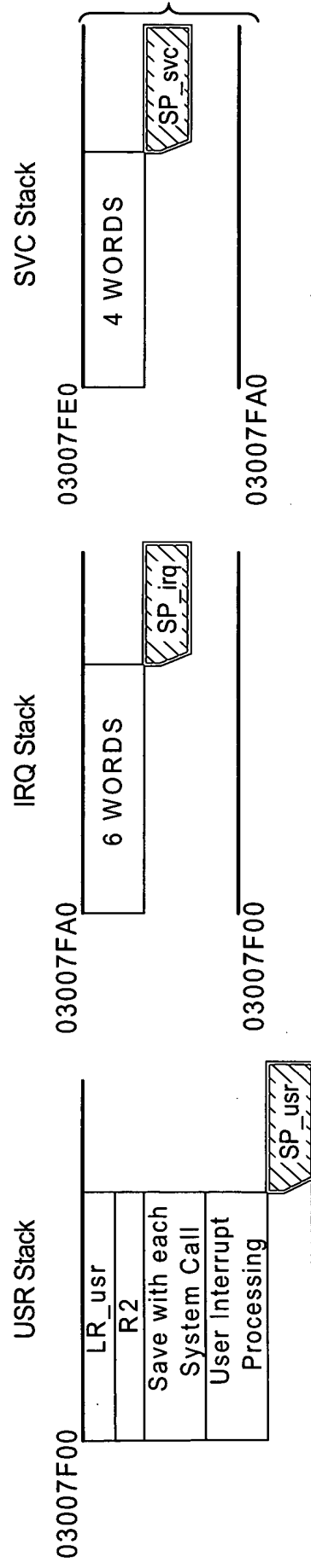


Fig. 128H

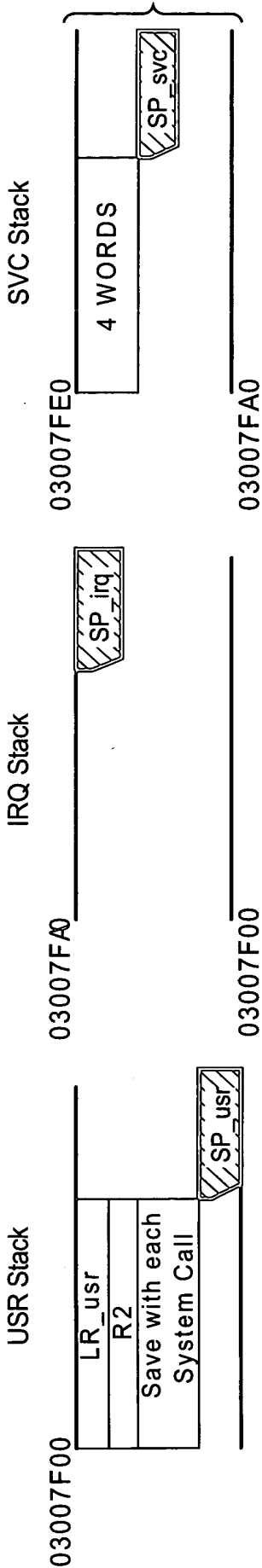


Fig. 128I

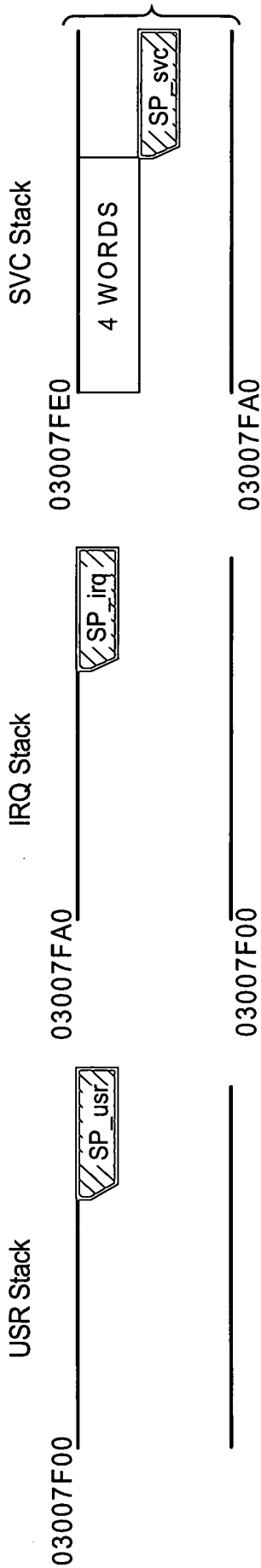


Fig. 128J

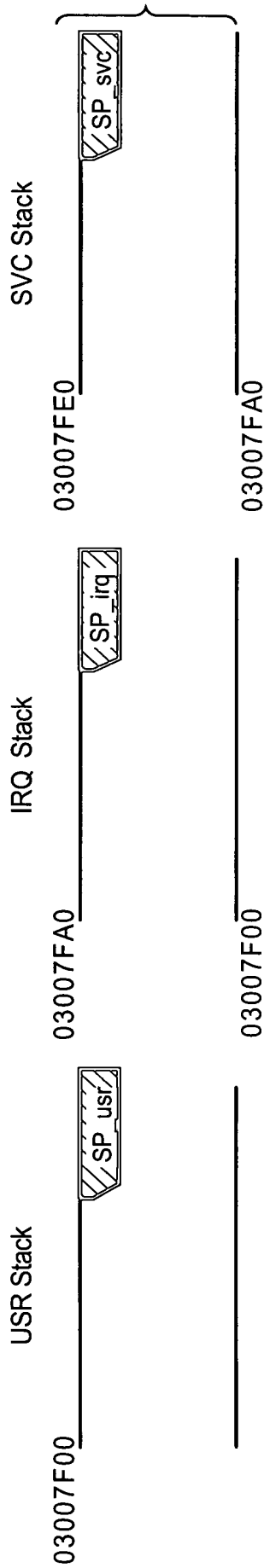


Fig. 128K

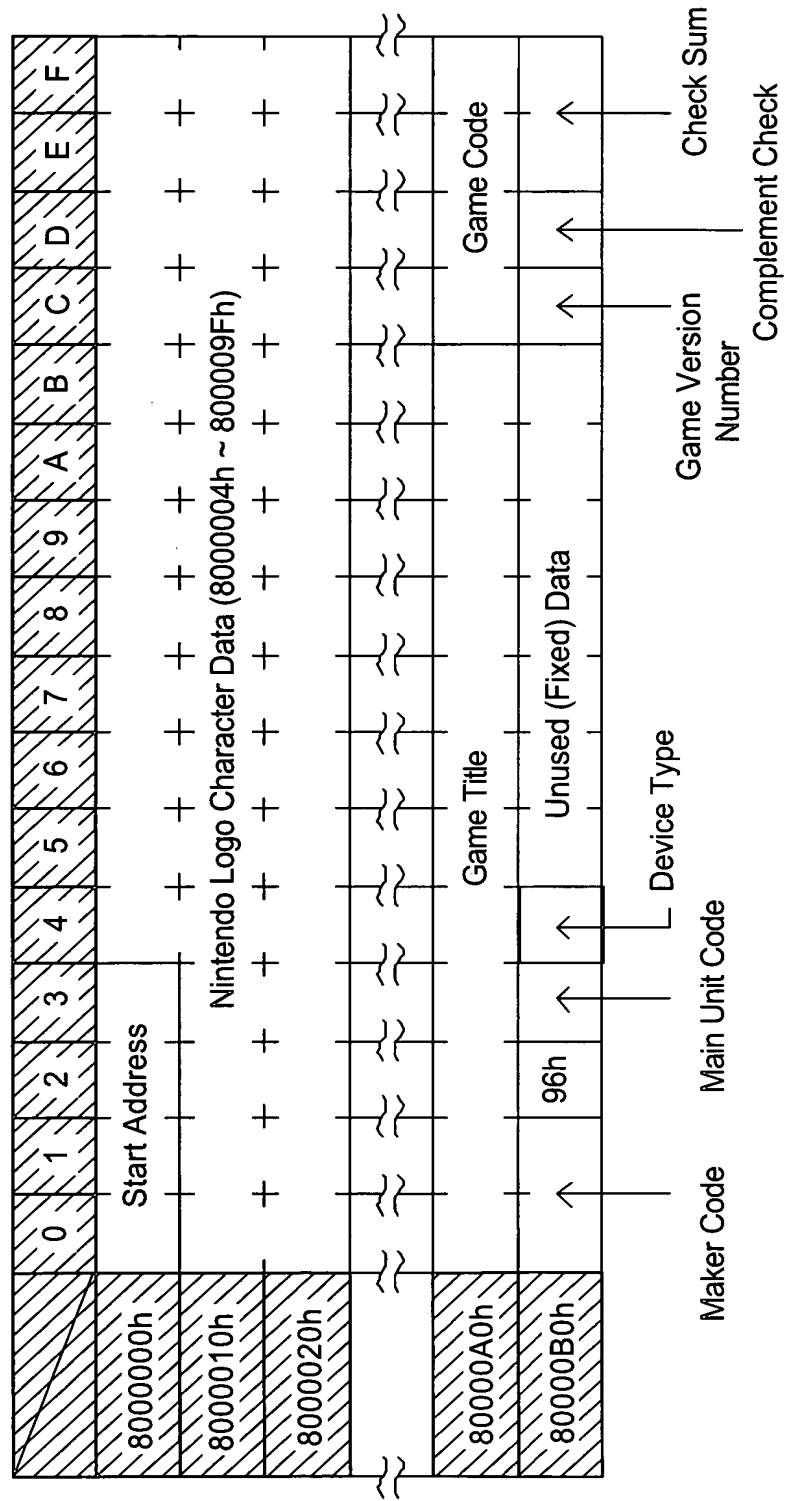
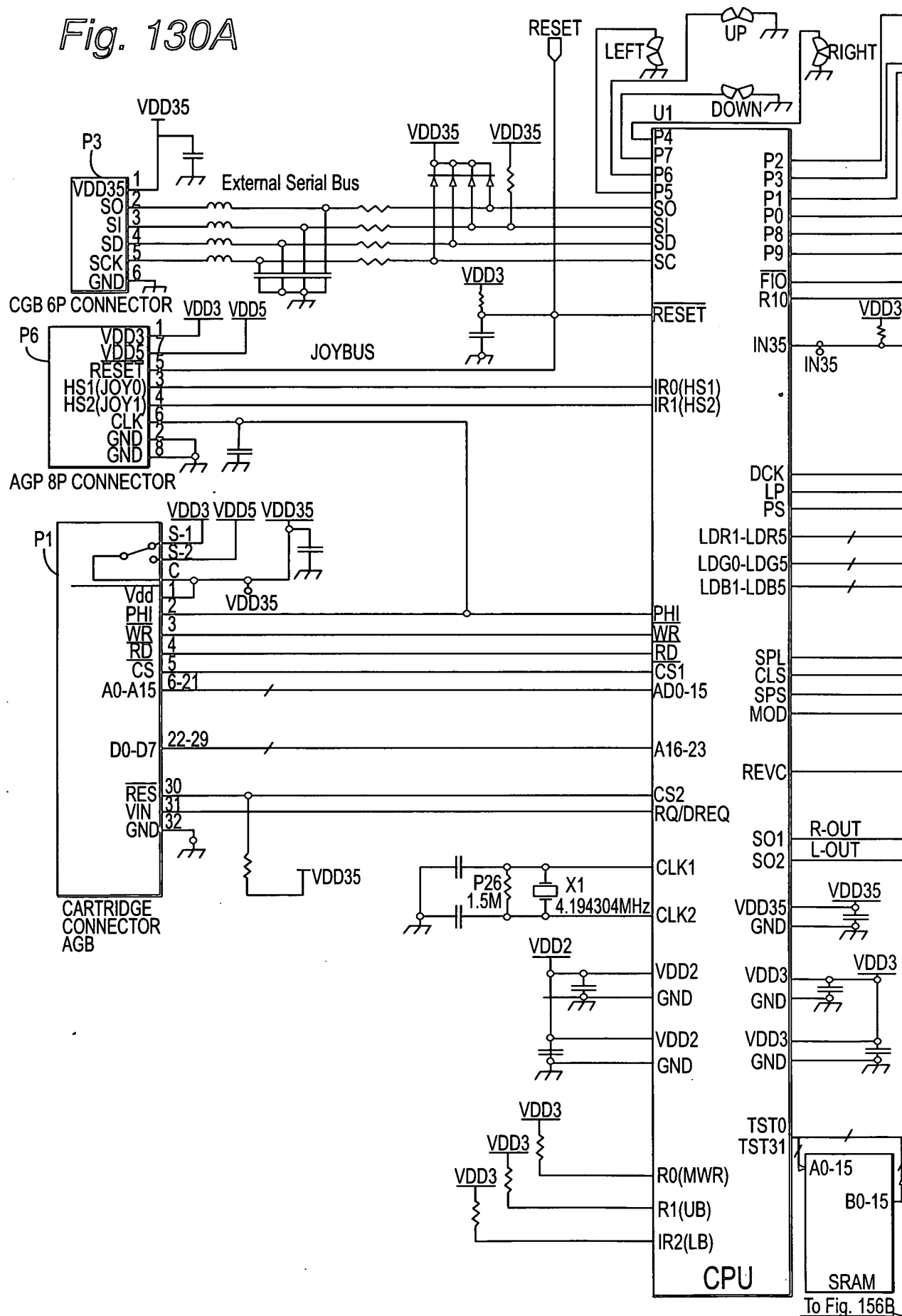


Fig. 129

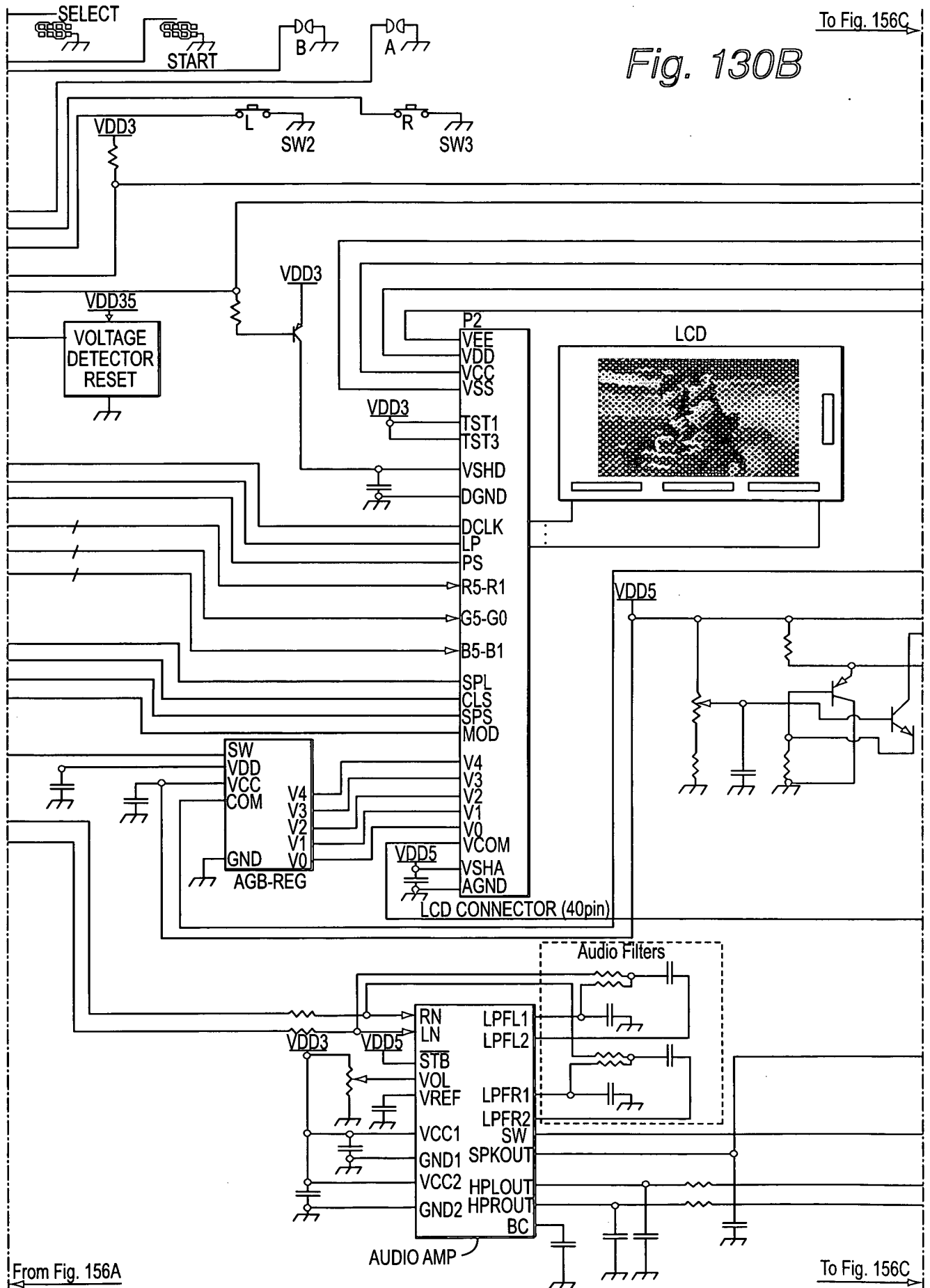
Fig. 130A



To Fig. 156B

Fig. 130B

To Fig. 156C

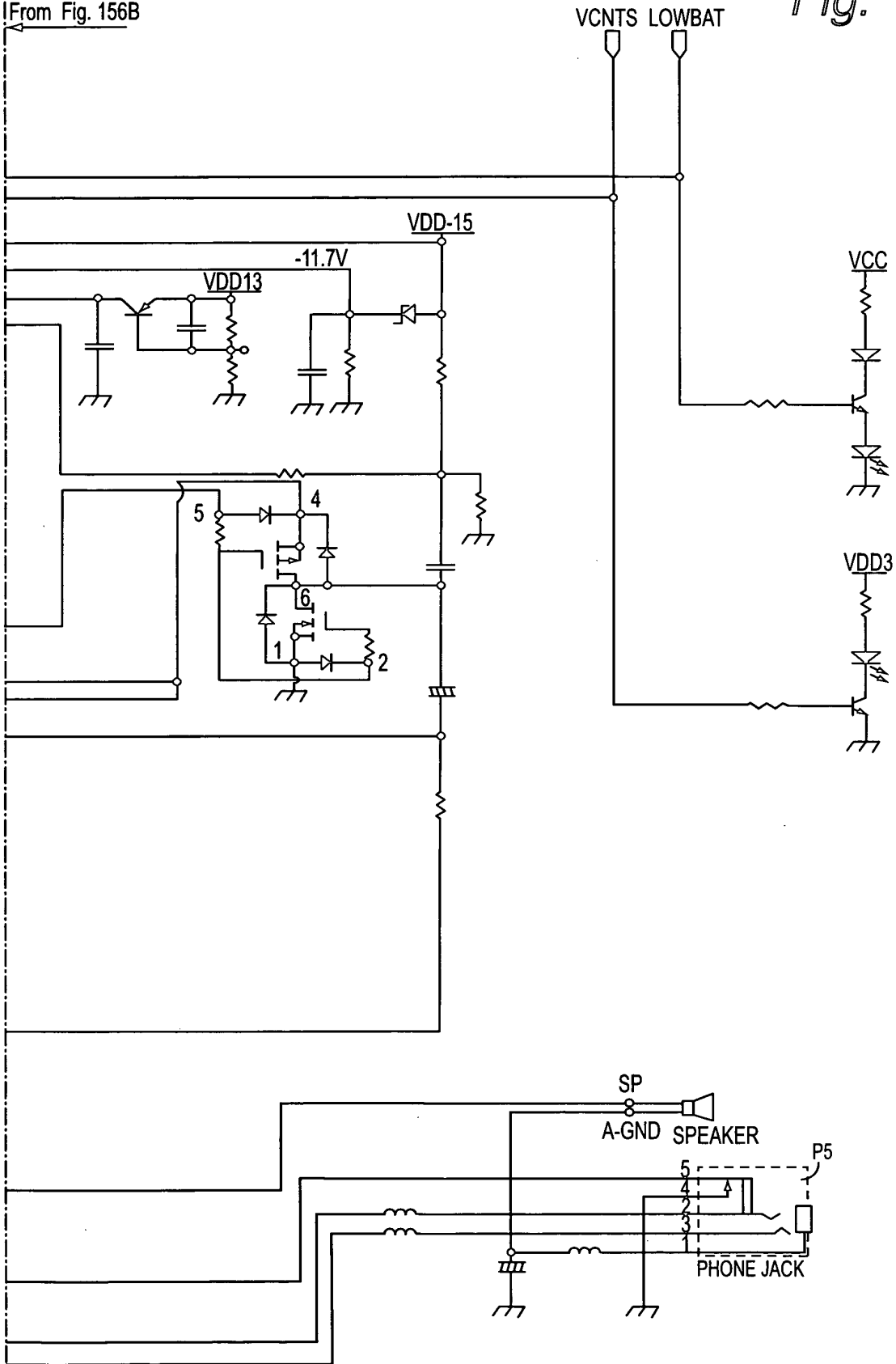


From Fig. 156A

To Fig. 156C

Fig. 130C

From Fig. 156B



From Fig. 156B

Addr		D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Figure in App.		
00	DISPCNT	Window Display Flag OBJWIN1WIN0		Display Flag OBJBG2BG3BG1BG0					Forced Blank	OBJ Map Format	OBJ J Hoff	Frame Buffer No.	CGB mode	BG Mode VBlank Counter EvalHBlank StatusVBlank Status			RW	0080h	Fig. 29			
04	DSPSTAT	V Count Setting				V Counter Match Interrupt				VBlank Interrupt	VBlank Interrupt						RW	0000h	Fig. 28			
06	VCOUNT	-	-	-	-	-	-	-	-		V Counter Value									R	0000h	Fig. 27
08	BG0CNT	Size		-	Screen Base Block					Color Mode	Mosaic	0	0	Character Base Block			Priority	RW	0000h	Fig. 32A		
0A	BG1CNT	Size		-	Screen Base Block					Color Mode	Mosaic	0	0	Character Base Block			Priority	RW	0000h	Fig. 32A		
0C	BG2CNT	Size		Area Overflow	Screen Base Block					Color Mode	Mosaic	0	0	Character Base Block			Priority	RW	0000h	Fig. 32B		
0E	BG3CNT	Size		Area Overflow	Screen Base Block					Color Mode	Mosaic	0	0	Character Base Block			Priority	RW	0000h	Fig. 32B		
10	BG0HOFs	-	-	-	-	-	-	-		Horizontal Offset										W	0000h	Fig. 45A
12	BG0VOFS	-	-	-	-	-	-	-		Vertical Offset										W	0000h	Fig. 45B
14	BG1HOFs	-	-	-	-	-	-	-		Horizontal Offset										W	0000h	Fig. 45A
16	BG1VOFS	-	-	-	-	-	-	-		Vertical Offset										W	0000h	Fig. 45B
18	BG2HOFs	-	-	-	-	-	-	-		Horizontal Offset										W	0000h	Fig. 45A
1A	BG2VOFS	-	-	-	-	-	-	-		Vertical Offset										W	0000h	Fig. 45B
1C	BG3HOFs	-	-	-	-	-	-	-		Horizontal Offset										W	0000h	Fig. 45A
1E	BG3VOFS	-	-	-	-	-	-	-		Vertical Offset										W	0000h	Fig. 45B
20	BG2PA	dx: Distance moved Along same line in x direction																		W	0100h	Fig. 44A
22	BG2PB	dmx: Distance moved Along next line in x direction																		W	0000h	Fig. 44B
24	BG2PC	dy: Distance moved Along same line in y direction																		W	0100h	Fig. 44C
26	BG2PD	dmy: Distance moved Along next line in y direction																		W	0000h	Fig. 44D

Fig. 131A

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	RW	Initial- Value in App	Fig. in App
28	BG2X_L	-																	0000h	Fig. 43A
2A	BG2X_H	-	-	-	-													W	0000h	Fig. 43B
2C	BG2Y_L																		0000h	Fig. 43C
2E	BG2Y_H	-	-	-	-													W	0000h	Fig. 43D
30	BG3PA																	W	0100h	Fig. 44A
32	BG3PB																	W	0000h	Fig. 44B
34	BG3PC																		0000h	Fig. 44C
36	BG3PD																	W	0100h	Fig. 44D
38	BG3X_L																		0000h	Fig. 43A
3A	BG3X_H	-	-	-	-													W	0000h	Fig. 43B
3C	BG3Y_L																		0000h	Fig. 43C
3E	BG3Y_H	-	-	-	-													W	0000h	Fig. 43D
40	WIN0H																	W	0000h	
42	WIN1H																	W	0000h	
44	WIN0V																	W	0000h	
46	WIN1V																	W	0000h	
48	WININ	-	-	Special Effects	OBJ	BG3	BG2	BG1	BG0	-	-	Special Effects	OBJ	BG3	BG2	BG1	BG0	RW	0000h	Fig. 65*
4A	WINOUT	-	-	Special Effects	OBJ	BG3	BG2	BG1	BG0	-	-	Special Effects	OBJ	BG3	BG2	BG1	BG0	RW	0000h	Fig. 66

Fig. 131B

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	RW	Initial- Value in App	Fig. in App				
4C	MOSAIC	OBJ Mosaic																	BG Mosaic			W	0000h	Fig. 35
		Vertical Size		Horizontal Size		Horizontal Size		Horizontal Size		Vertical Size		Horizontal Size												
50	BLDMOD	-	-	BD	OB J	BG 3	BG 2	BG 1	BG 0	Type of Color Special Effect		BD	OB J	BG 3	BG 2	BG 1	BG 0	RW	0000h	Fig. 67				
52	COLEV	-	-	-	Color Special Effect Coefficient EVB				-	-	-	-	Color Special Effect Coefficient EVA						0000h	Fig. 68A				
54	COLEY	-	-	-	-	-	-	-	-	-	-	-	Color Special Effect Coefficient EVY					W	0000h	Fig. 68B				
60	SG10_L	-	-	-	-	-	-	-	-	NR1 0									W/R	0000h	Fig. 72A			
62	SG10_H	NR12																	W/R	0000h	Fig. 72B			
64	SG11	NR14																	W/R	0000h	Fig. 72C			
68	SG20	NR22																	W/R	0000h	Fig. 74A			
6C	SG21	NR24																	W/R	0000h	Fig. 74B			
70	SG30_L	-	-	-	-	-	-	-	-	NR3 0									W/R	0000h	Fig. 75A			
72	SG30_H	NR32																	W/R	0000h	Fig. 75B			
74	SG31	NR34																	W/R	0000h	Fig. 75C			
78	SG40	NR42																	W/R	0000h	Fig. 77A*			
7C	SG41	NR44																	W/R	0000h	Fig. 77B			
80	SGCNT0_L	NR51																	W/R		Fig. 78A			
82	SGCNT0_H	FIFO B reset		TIMER		L Output		R Output		FIFO A reset		TIMER		L Output		R Output		W/R	0000h	Fig. 78C				
84	SGCNT1	-	-	-	-	-	-	-	-	-	-	-	-	DSB Output Ratio	DSA Output Ratio	Sound 1-4 Mix Ratio		W/R	0000h	Fig. 78B				
88	SGBIAS	Amplitude Resolution/ Sampling Cycle		-		-		-		-		-		NR5 2				W/R	0000h	Fig. 78B				
		Bias Level																	W/R	0000h	Fig. 79			

Fig. 131C

Fig.
131D

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App.		
90	SGWR0_L	Step 2			Step 3			Step 0			Step 1			W/R			-	Fig. 76A				
92	SGWR0_H	Step 6			Step 7			Step 4			Step 5			W/R			-	Fig. 76B				
94	SGWR1_L	Step 10			Step 11			Step 8			Step 9			W/R			-	Fig. 76C				
96	SGWR1_H	Step 14			Step 15			Step 12			Step 13			W/R			-	Fig. 76D				
98	SGWR2_L	Step 18			Step 19			Step 16			Step 17			W/R				Fig. 76E				
9A	SGWR2_H	Step 22			Step 23			Step 20			Step 21			W/R			-	Fig. 76F				
9C	SGWR3_L	Step 26			Step 27			Step 24			Step 25			W/R			-	Fig. 76G				
9E	SGWR3_H	Step 30			Step 31			Step 28			Step 29			W/R			-	Fig. 76H				
A0	SGFIFOA_L	Sound Data 1			Sound Data 0			W			-			Fig. 71A								
A2	SGFIFOA_H	Sound Data 3			Sound Data 2			W			-			Fig. 72A								
A4	SGFIFOB_L	Sound Data 1			Sound Data 0			W			-			Fig. 71A								
A6	SGFIFOB_H	Sound Data 3			Sound Data 2			W			-			Fig. 72A								
B0	DM0SAD_L	W																		0000h	Fig. 82A	
B2	DM0SAD_H	-	-	-	-	-	-	W											0000h	Fig. 82B		
B4	DM0DAD_L	W																		0000h	Fig. 83A	
B6	DM0DAD_H	-	-	-	-	-	-	W											0000h	Fig. 83B		
B8	DM0CNT_L	-	-	W															Fig.84			
BA	DM0CNT_H	DMA 0 Control																		W/R	0000h	Fig.85
		Enable	Interrupt	Startup Timing	-	Transfer Width	Continuous	Source Address Control	Destination Address Control	-	-	-	-	-	-	-	-	-	-			

Fig. 131E

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	RW	Initial-Value in App.	Fig.					
BC	DM1SAD_L	DMA 1 Source Address																		W	0000h	Fig. 86A			
BE	DM1SAD_H	-	-	-	-	-	-	DMA 1 Source Address											W	0000h	Fig. 86B				
C0	DM1DAD_L	DMA 1 Destination Address																		W	0000h	Fig. 87A			
C2	DM1DAD_H	-	-	-	-	-	-	DMA 1 Destination Address											W	0000h	Fig. 87B				
C4	DM1CNT_L	-	-	Word Count														W		Fig. 88					
C6	DM1CNT_H	DMA 1 Control																		W/R	0000h	Fig. 89			
C8	DM2SAD_L	Enable	Interrupt	Startup timing	-	Transfer Width	Contin-uous	Source Address Control	Destination Address Control										-	-	-	-	W	0000h	Fig. 86A
CA	DM2SAD_H	-	-	-	-	DMA 2 Source Address													W	0000h	Fig. 86B				
CC	DM2DAD_L	DMA 2 Destination Address																		W	0000h	Fig. 87A			
CE	DM2DAD_H	-	-	-	-	-	-	DMA 2 Destination Address											W	0000h	Fig. 87B				
D0	DM2CNT_L	-	-	Word Count														W		Fig. 88					
D2	DM2CNT_H	DMA 2 Control																		W/R	0000h	Fig. 89			
D4	DM3SAD_L	Enable	Interrupt	Startup timing	-	Transfer Width	Contin-uous	Source Address Control	Destination Address Control										-	-	-	-	W	0000h	Fig. 90A
D6	DM3SAD_H	-	-	-	-	DMA 3 Source Address													W	0000h	Fig. 90B				
D8	DM3DAD_L	DMA 3 Destination Address																		W	0000h	Fig. 91A			
DA	DM3DAD_H	-	-	-	-	-	-	DMA 3 Destination Address											W	0000h	Fig. 91B				
DC	DM3CNT_L	Word Count																		W	0000h	Fig. 92			
DE	D3CNT_H	DMA 3 Control																		W/R	0000h	Fig. 93			
		Enable	Interrupt	Startup timing	DREQ	Transfer Width	Contin-uous	Source Address Control	Destination Address Control										-	-	-	-	-		

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	RW	Initial-Value	Fig. in App.		
100	TM0D	Timer 0 Setting																		W	0000h	Fig. 81A
		Timer 0 Control																				
102	TM0CNT	Operation	Interrupt	.	.	.	Count Up Timing	Prescaler		RW	0000h	Fig. 81B		
104	TM1D	Timer 1 Setting																		W	0000h	Fig. 81A
		Timer 1 Control																				
106	TM1CNT	Operation	Interrupt	.	.	.	Count Up Timing	Prescaler		RW	0000h	Fig. 81B		
108	TM2D	Timer 2 Setting																		W	0000h	Fig. 81A
		Timer 2 Control																				
10A	TM2CNT	Operation	Interrupt	.	.	.	Count Up Timing	Prescaler		RW	0000h	Fig. 81B		
10C	TM3D	Timer 3 Setting																		W	0000h	Fig. 81A
		Timer 3 Control																				
10E	TM3CNT	Operation	Interrupt	.	.	.	Count Up Timing	Prescaler		RW	0000h	Fig. 81B		

Fig. 131F

Addr	Register	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	R/W	Initial-Value	Fig. in App.	
120	SCD0	32-Bit Normal SIO Communication Data and Multi-play Communication Data 0																		Fig. 97A	
122	SCD1	32-Bit Normal SIO Communication Data and Multi-play Communication Data 1																		Fig. 97B	
124	SCD2	Multi-play Communication Data 2																		Fig. 104C	
126	SCD3	Multi-play Communication Data 3																		Fig. 104D	
128	SCCNT_L	Port Control				SIO Control															
	Normal SIO Communication	-	Interrupt Enable	0	Transfer Bit Length	-	-	-	-	Start	-	-	-	Transfer Enable Flag Send	Transfer Enable Flag Receive	Shift Clock Freq.	Shift Clock	R/W	0000h	Fig. 98	
	Multi-play Communication	-	Interrupt Enable	1	0	-	-	-	-	Start (master Busy (slave))	Communication Error Flag	Multi-play ID		SD Terminal Monitor	SI Terminal Monitor	Baud Rate		R/W	0000h		
	UART Communication	-	Interrupt Enable	1	1	Receive Enable Flag	Send Enable Flag	Parity Enable Flag	FIFO Enable Flag	Data Length	Error Flag	Receive Data Flag	Send Data Flag	Parity Control	CTS Flag	Baud Rate		R/W	0000h		
12A	SCCNT_H	Communication Data																		Fig. 96	
	Normal SIO Communication	-	-	-	-	-	-	-	-	-	-	8Bit Normal SIO Communication Data								R/W	0000h
130	P1	-	-	-	-	-	-	L	R	Down	Up	L	R	Start	Select	B	A	R/W	0000h	Fig. 119	
132	P1CNT	Interrupt Conditions	Interrupt Enable	-	-	-	-	L	R	Down	Up	L	R	Start	Select	B	A	R/W	0000h	Fig. 120	
134	R	Communication Function Select	-	-	-	-	-	-	Interrupt Enable	SO	SI	SD	SC	SO	SI	SD	SC	R/W	0000h	Fig. 109	

Fig. 131G

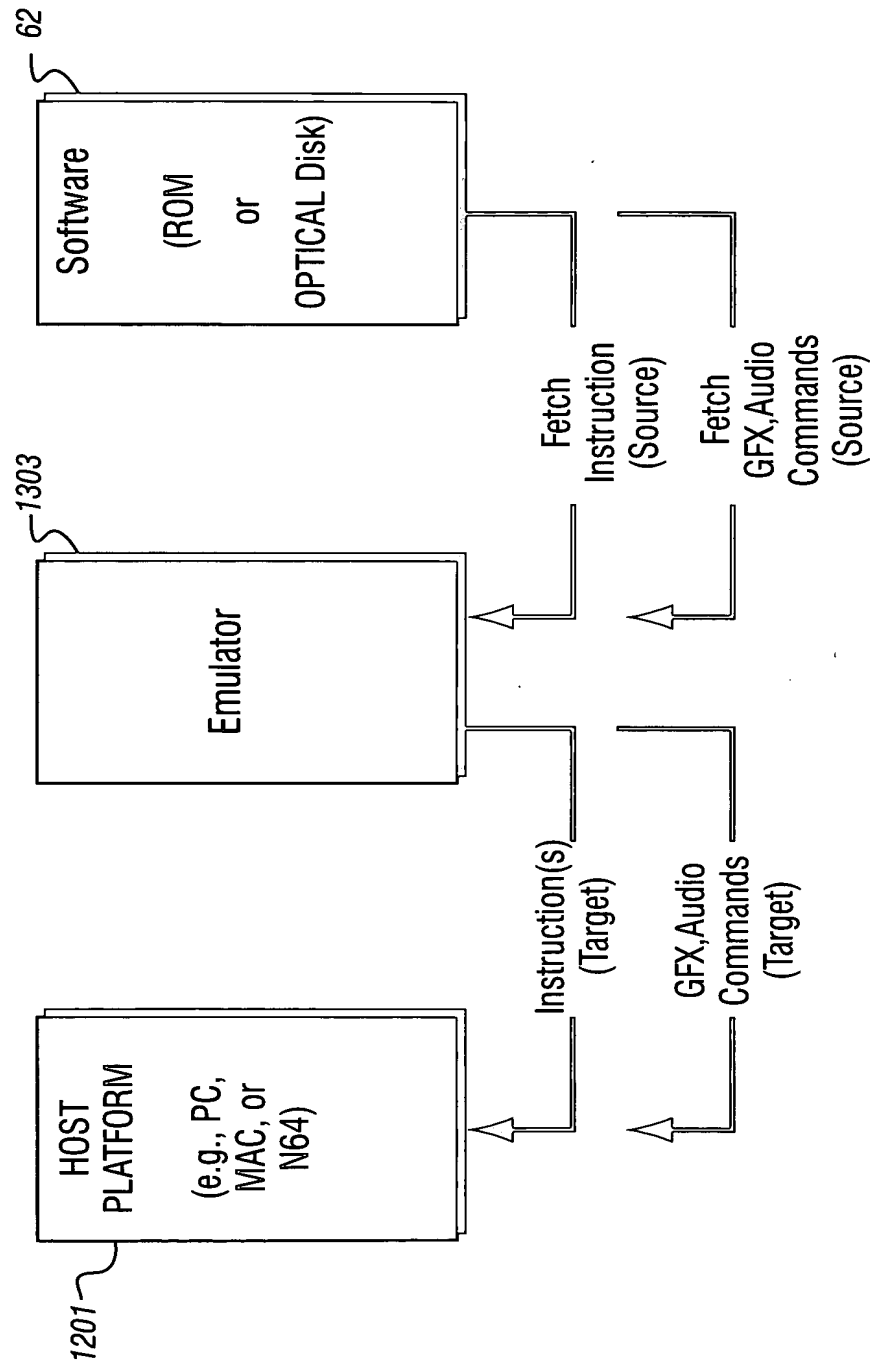
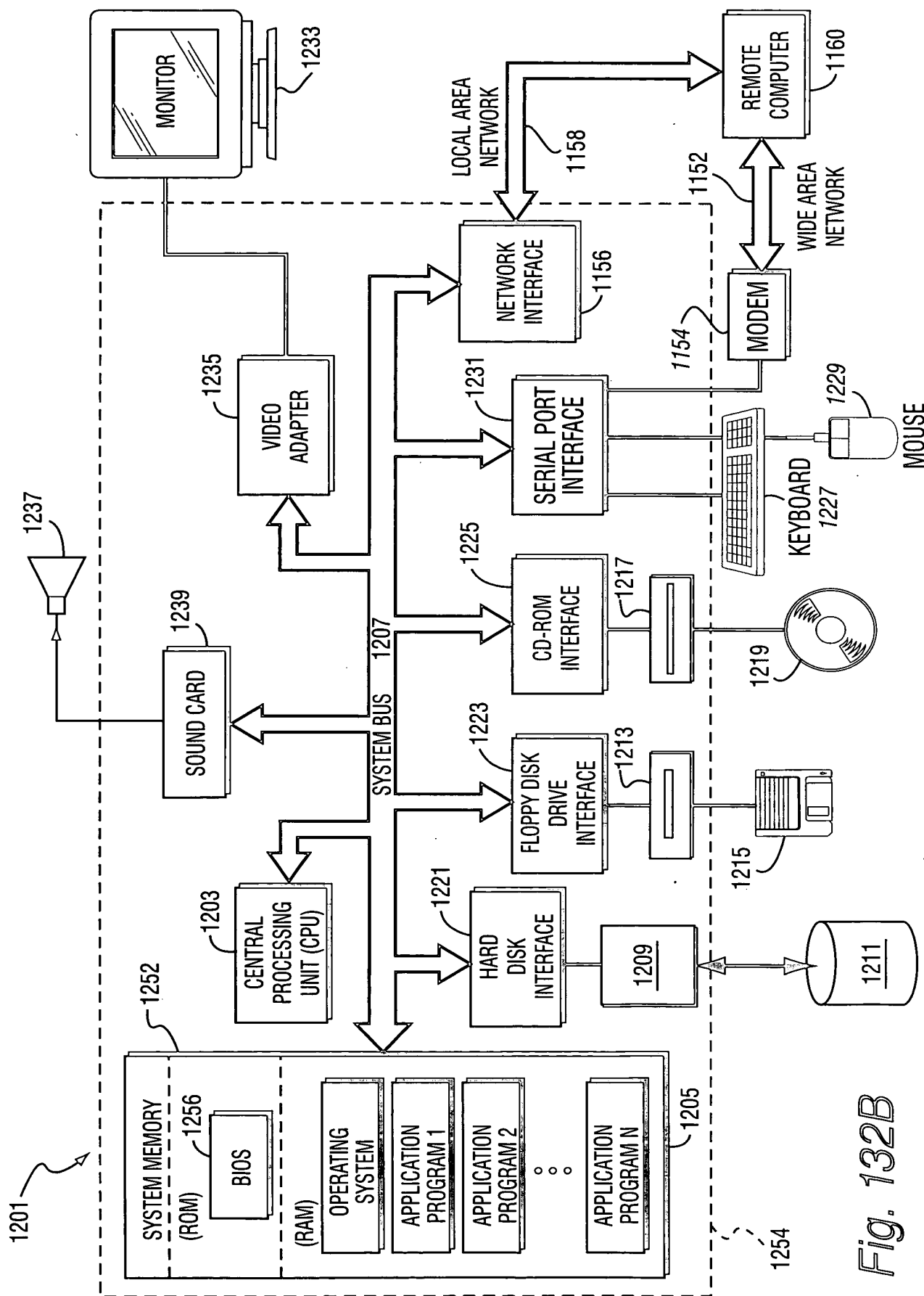


Fig. 132A



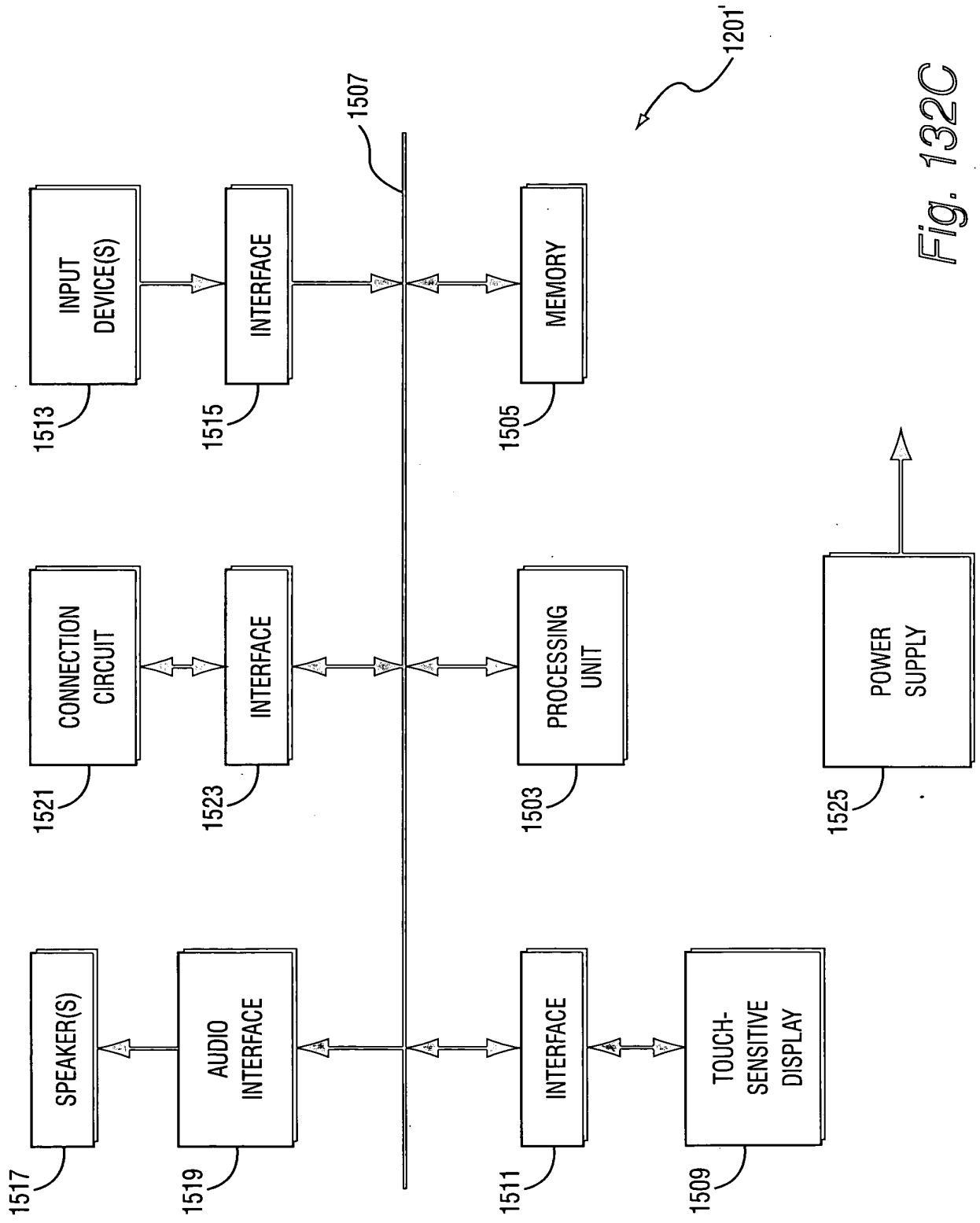


Fig. 132C

